

APPLICATION NOTE

ANS022 | Bridge capacitor for isolated power modules, the whole truth, no myths

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1. INTRODUCTION

Deciding which type of common mode EMC filter to choose when designing an isolated DC/DC converter or a power module to pass the EMC test still often leads to less-than-optimal solutions. Knowledge about common mode interference and its minimisation is characterised by myths. 'Common mode interference is quite difficult to understand' is the first argument put forward. Followed by 'common mode interference is more of a trial-and-error process'. A common mode choke is almost exclusively cited as the method of choice for minimisation. However, this way of looking at things neglects the fact that common mode interference can also be explained with the help of basic electrical interactions or parasitic elements and Kirchhoff's law. The purpose of this article is to provide a basis for understanding the origin and propagation of common-mode interference and an approach based on a formula for designing a simple filter to minimise common-mode interference.

Unlike non-isolated DC/DC converters, such as a buck converter, an isolated DC/DC converter has common mode interference in addition to differential mode interference. Comparison of interference types can be seen from Table 1.

In the event of differential mode interferences, the interference current in the supply lines always flows in the opposite direction between the power supply and the power module. It is essentially the switched input current.

As can be seen in Figure 1, the interference current flows through the interwinding capacitance C_K .

The return path of the common mode current is via the earth path through the parasitic coupling capacitance C_P .

If you now look at the path of the interference current, it appears to close via the 'air'. In reality, however, it is the current through the stray capacitance (power module structure, lines to reference ground) of the arrangement, which is shown here as capacitor C_P .

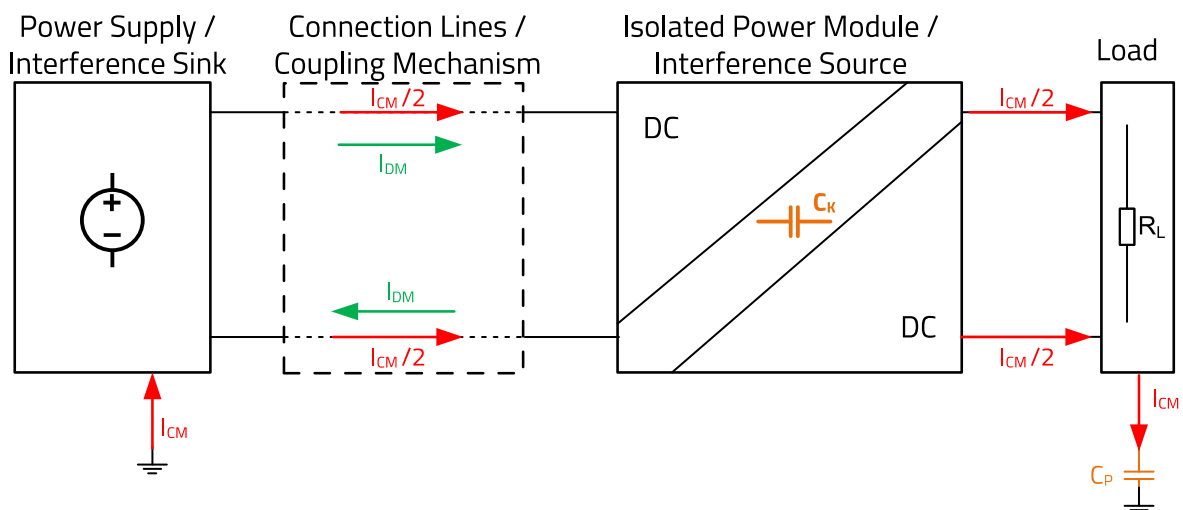


Figure 1: Basics of differential and common mode interference.

Differential mode disturbances (I_{DM})	Common mode disturbances (I_{CM})
Current in the supply lines in the opposite direction	Current in the supply lines in the same direction
Same orientation as the input current from the power module	Mainly due to a high du/dt of the switching elements
Dominant with non-isolated power modules	Occurs mainly with isolated power modules

Table 1: Comparison of interference types.

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2. MAGI³C POWER MODULE AND EMC ENVIRONMENT

Isolated power modules are used in many industrial applications. Be it as a supply for an RS485 interface or for sensor data acquisition. Due to the wide range of possible applications and the resulting different environmental conditions, i.e. different C_P 's, we use a standardised structure based on CISPR 16-2-1 to ensure that the filters can be compared with each other.

2.1 Test setup based on CISPR 16-2-1

Figure 2 illustrates the setup that forms the basis for the tests in this article.

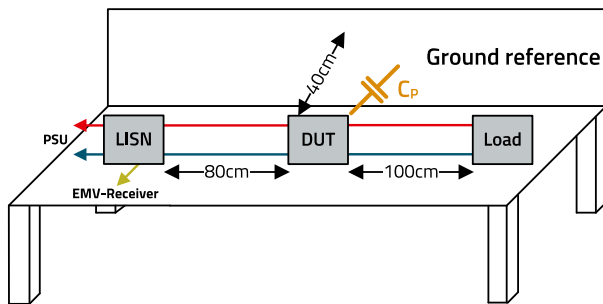


Figure 2: EMC test setup based on CISPR 16-2-1.

The setup shows the essential components that are necessary for a conducted measurement of the interference voltage. A detailed description of the measurement setup in accordance with CISPR 16-2-1 can be found in the Support Note [SN023 | Conducted emissions test](#).

The device under test (DUT) is a Magi³C evaluation board with a size of 80 × 80 mm. The coupling capacitance in Figure 2 is representative of the

- parasitic capacities of the DUT for ground reference
 - parasitic capacitance of the load to ground reference
 - parasitic capacitance of the load lines to the ground reference
- } C_P

The coupling capacitance to the environment (ground reference) forms the path for the common mode current to close the circuit. However, the impedance of the capacitance is not a fixed value but varies with the frequency. This is clearly reflected in the formula for the capacitive reactance $|X_C|$:

$$|X_C| = \frac{1}{\omega \cdot C} = \frac{1}{2 \cdot \pi \cdot f \cdot C} \quad (1)$$

ω – K Circular frequency [Hz]

C – Capacitance [F]

f – Frequency [Hz]

The following two subsections present methods for determining the value of the coupling capacitance C_P . For clarification, the respective values are determined using a numerical example that corresponds to the structure used in this article. Both methods are approximations and cannot provide an exact value due to the complexity of the real structure of a coupling capacitance.

Figure 3 shows the structure and the power module (evaluation board) with the components that are relevant for the common mode analysis.

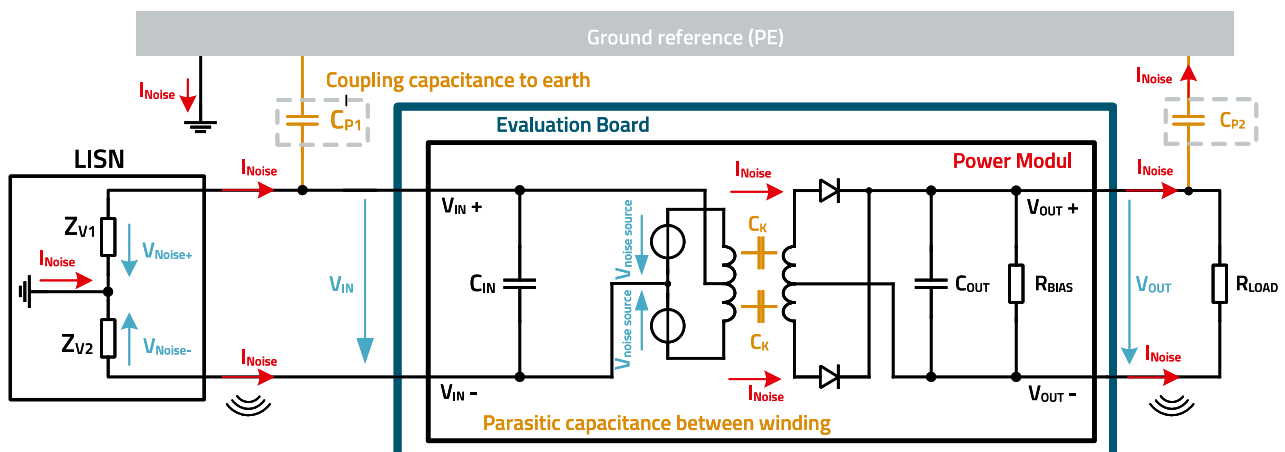


Figure 3: Schematic measurement setup based on CISPR-16-2-1.

The switching elements on the primary side of the power module are the source of the common mode interference. The switched voltage V_{noise} drives a current I_{noise} through the intermediate winding capacitance C_K of the transformer to the secondary side of the power module. The interference currents propagate via the output lines and flow via the coupling capacitance C_{P2} to the earth reference (PE). The circuit to the input of the evaluation board is then closed via the earth reference and C_{P1} . The output and input lines also act as antennas, which leads to the 'radiation' of parts of the interference current I_{noise} .

2.2 The coupling capacitance C_P to the environment - theoretical determination via the geometry

The areas and geometries of different potentials and their distance from each other are decisive for the formation of a parasitic capacitance. In the case under consideration, the DUT consists of an evaluation board (EVB) with an area of $80 \times 80 \text{ mm}$, whereby the insulated module used is operated with a resistive load. The output cables used to the load have a length of 100 cm and the distance to the measuring plate (ground reference) is 40 cm . Two cases must therefore be considered when determining the coupling capacitance C_P . Case 1, the coupling of the evaluation board to the measuring plate and Case 2, the coupling of the output lines to the measuring plate, as shown in Figure 3.

This allows us to use the two cases shown in Figure 3 and calculated in Figure 4 as a basis for determining the coupling capacitance. The influence of the ohmic load, in this case represented by a sliding resistor, was not taken into account.

2.3 The coupling capacitance C_P to the environment - metrological determination via the resonance

A metrological approach is to connect a defined inductance in series with the coupling capacitance to the environment and thus create a series resonant circuit. The required C_P can then be calculated using the frequency at resonance and the formula for the series resonant circuit.

The size of the inductance inserted is determined by the existing inductance values such as transformer, cables, copper tracks etc. For the power module we are looking at here, we have inserted a **PD2** inductance of $15 \mu\text{H}$ into both the positive and negative lines of the power module input. It is important here not to select an inductance value that is too high, as otherwise the inductance would influence the power module and therefore no measurement would take place during normal operation. On the other hand, the inductance must be large enough in relation to the line inductances so that these can be neglected in the analysis.

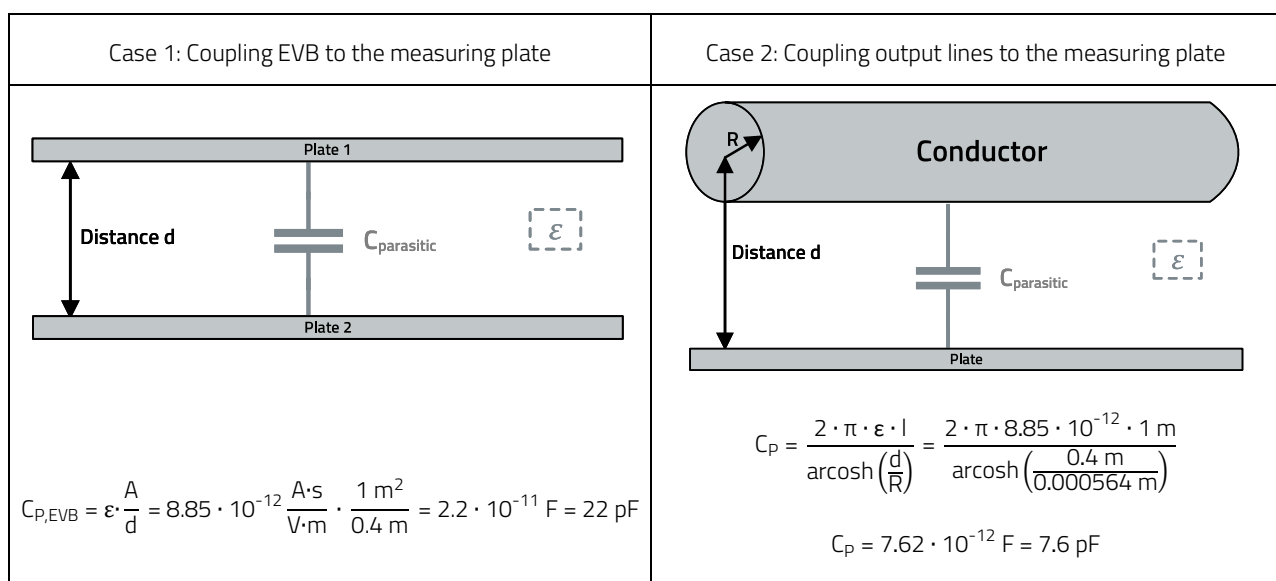


Figure 4: Examples of coupling capacities.

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Analysing the measurements in Figure 5 shows that there is a resonance point at approx. 15 MHz.

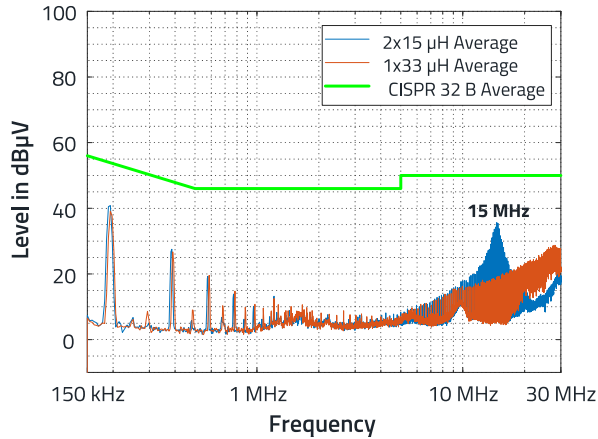


Figure 5: EMC plot with resonance point of the conducted interference voltage.

The value of the parasitic capacitance can be calculated using the resonance frequency and the inserted inductance. Due to the output capacitance, both output lines are at the same potential in the high-frequency range so that they can be considered together as a single line for the calculation. The total inductance L corresponds to the parallel connection of the two 15 μH inductors introduced, resulting in a value of 7.5 μH for the calculation of the parasitic capacitance.

The formula for the series resonant circuit, converted to C_P , provides the required value:

$$C_P = \frac{1}{L \cdot (2 \cdot \pi \cdot f_{\text{res}})^2} \quad (2)$$

$$C_P = \frac{1}{7.5 \cdot \mu\text{H} \cdot (2 \cdot \pi \cdot 15 \text{ MHz})^2} = 15 \text{ pF} \quad (3)$$

The first estimate of the C_P with 22 pF based purely on the geometric view, see Figure 4: Case 1, is therefore sufficiently accurate. The deviation from the value determined by measurement is due to the influence of the load and the structure itself.

3. COMMON MODE INTERFERENCE SUPPRESSION WITH BRIDGE CAPACITOR

3.1 The intention of filtering

The most elegant way to pass the EMC test is to prevent interference, in this case common mode interference, from reaching the network simulator (LISN) in the first place. For an isolated power module, this means that the interference current is diverted past the LISN. But what does this mean for the case under consideration here? Figure 6 is a simplified representation of the real set-up as already shown in Figure 3. The figure illustrates the fundamentals on which the derivation of the equation is based.

Figure 6 shows both (path 1 & path 2) interference current loops. Path 2, marked in red, illustrates the path of the common mode interference current that flows through the power module via C_K and closes its circuit via earth.

Path 1, marked in blue here, shows an alternative loop. The current flows through the power module and then makes an

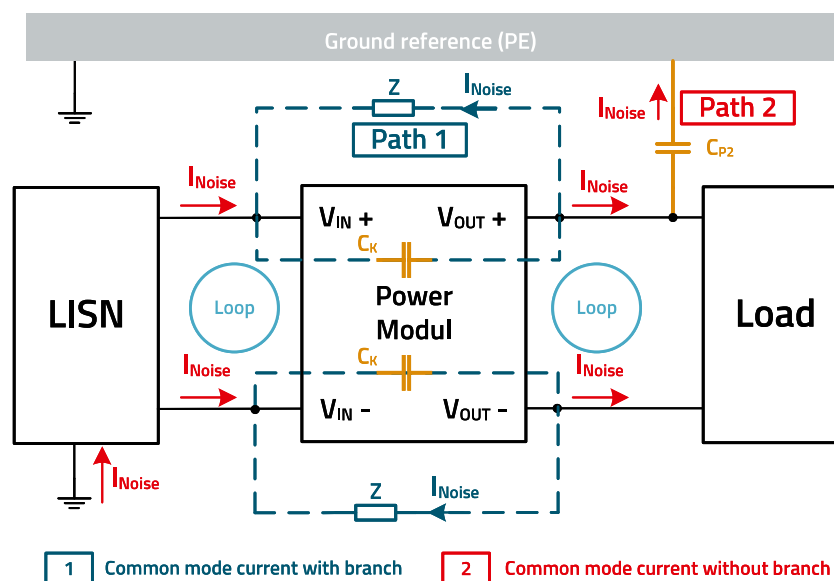


Figure 6: Equivalent circuit diagram with representation of the interference currents.

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'arc around the power module'. The interference current thus flows past the LISN.

To summarise, this means:

- Interference current circulates within the power module and cannot flow into the surrounding system.
- No interference current through the LISN means no interference potential at the LISN.

But why should the interference current choose the branch?

Path 1 must be more 'attractive' for I_{Noise} than path 2, i.e. it must have a lower impedance than path 2. This means that only a capacitor can be considered as a component, see Formula 1.

Path 1 is therefore the resulting interference loop in and around the power module.

The equivalent circuit diagram can now be extended by a real component for the branch as follows.

The equivalent circuit diagram shown in Figure 7 has already been expanded to include the required elements, as it forms the basis for the subsequent determination of the equations.

The input and output capacitances of the power module, shown in grey, balance, i.e. distribute the common mode interference currents so that only one C_Y is required instead of two.

3.2 EMC meets Kirchhoff's law

In order to determine the efficiency of the measure with the Y-capacitor, the circuit without the junction should be compared with the circuit with the implemented junction. In other words, we compare the voltage drop of the interference current at the LISN with bridge capacitor with the voltage drop without bridge capacitor. The ratio, expressed in dB, is then the attenuation a (Figure 8).



Figure 7: Basic concept for calculating damping.

In this case, the configuration without Y capacitor (amplitude A_1) is compared with the configuration with Y capacitor (amplitude A_2):

- Damping $a = a_2 - a_1$ in dB.
- Damping $a = 20 \cdot \log(\text{Voltage drop across LISN with bridge capacitor}) - 20 \cdot \log(\text{Voltage drop across LISN without bridge capacitor})$ dB.
- Damping $a = 20 \cdot \log\left(\frac{\text{Voltage drop across LISN with bridge capacitor}(V_2)}{\text{Voltage drop across LISN without bridge capacitor}(V_1)}\right)$ dB

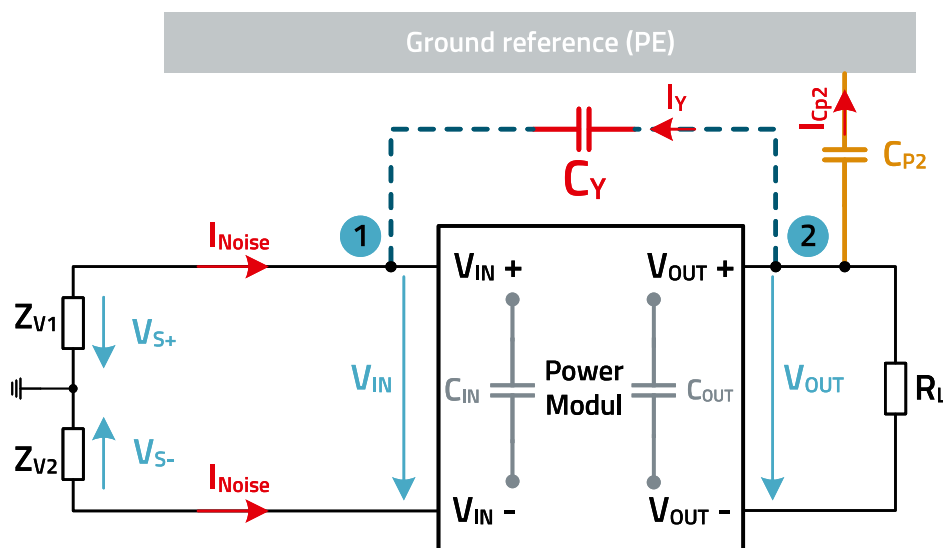


Figure 8: Equivalent circuit diagram with capacitive branching of the common-mode fault.

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For the further calculation, the factor A is introduced, which represents the ratio of 'voltage drop at the LISN with bridge capacitor' to 'voltage drop at the LISN without bridge capacitor'.

$$A = \frac{V_2}{V_1} \quad (4)$$

To determine the value of the bridge capacitor, we must now convert the known circuit diagram into a simplified electrical equivalent circuit diagram, to which we can then apply Kirchhoff's law. Kirchhoff's law consists of two basic rules: The node rule (1st Kirchhoff's law) states that in a node the sum of the incoming currents is equal to the sum of the outgoing currents. The mesh rule (2nd Kirchhoff's law) states that the sum of the voltages in a closed loop is equal to zero (Figure 9 and Figure 10).

A simplified equivalent circuit diagram can be created from the illustrations. Here, the supply lines to the power module are simplified to a single line corresponding to the parallel connection. Z_V represents the two impedances Z_{V1} and Z_{V2} of the LISN. The impedance of the parasitic coupling capacitance between the primary and secondary side of the transformer in the power module is the impedance Z_K . The capacitance $CP2$ represents the total parasitic capacitance on the secondary side and applies equally to both lines. V_S represents all common mode interference voltage sources in the power module, see figure 3 V_{noise} source. Z_Y is the impedance of the bridge capacitor that connects V_{OUT+} to V_{IN+} and is parallel to the impedance Z_K .

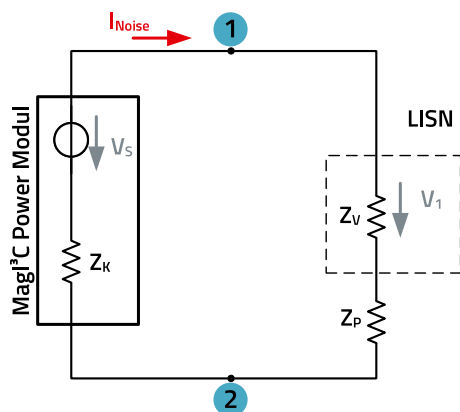


Figure 9: Equivalent circuit diagram, voltage drop without bridge capacitor.

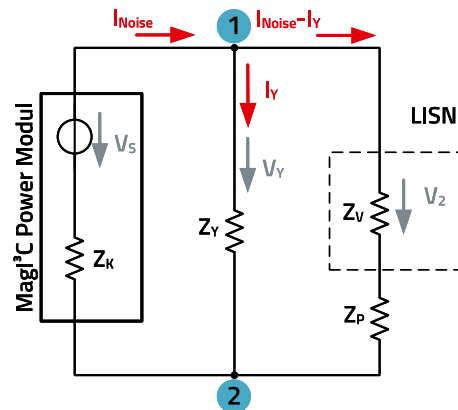


Figure 10: Equivalent circuit diagram, voltage drop with a bridge capacitor of impedance Z_Y .

Voltage drop without bridge capacitor:

The LISN, the parasitic capacitance and the Magl³C power module are connected in series here. We can therefore calculate V_1 using the familiar formula for a voltage divider. If we now rearrange the basic equation for the series connection according to the voltage V_1 we are looking for, we obtain the following equation, which represents the voltage drop across the LISN.

$$V_1 = V_S \cdot \frac{Z_V}{Z_K + Z_P + Z_V} \quad (5)$$

V_1, V_2 – Voltage drop across the LISN

Z_K – Impedance of the winding capacitance

Z_P – Impedance of the parasitic coupling capacitance

Z_V – Impedance of the LISN

V_Y – Voltage drop across the bridge capacitor

Z_Y – Impedance of the bridge capacitor

V_S – Common-mode interference voltage source

Voltage drop with bridge capacitor:

In the following, the circuit is a mixture of a series and a parallel circuit. Z_Y , the bridge capacitor, is connected in parallel with the LISN and the parasitic capacitance. The parallel branch is then connected in series with the Magl³C power module.

If we now rearrange the basic equation for the parallel circuit and the series circuit according to the voltage V_2 we are looking for, we obtain the equation that represents the voltage drop across the LISN when the bridge capacitor is implemented.

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$$V_2 = V_S \cdot \frac{Z_Y}{Z_K + Z_Y \parallel (Z_V + Z_P)} \cdot \frac{Z_V}{Z_P + Z_V} \quad (6)$$

V_1, V_2 – Voltage drop across the LISN

Z_P – Impedance of the parasitic coupling capacitance

Z_V – Impedance of the LISN

V_Y – Voltage drop across the bridge capacitor

If we now insert the equation for V_1 and V_2 into the damping equation, we obtain the required expression.

$$A = \frac{Z_Y \cdot (Z_K + Z_P + Z_V)}{(Z_K + Z_Y \parallel (Z_V + Z_P)) \cdot (Z_V + Z_P)} \quad (7)$$

This equation can be further simplified for our purposes.

Chapter 5.1 shows the exact derivation for the simplification and the expected error using a numerical example.

$$A = \frac{Z_Y}{Z_K} \quad (8)$$

$$\text{Damping } a = 20 \cdot \log \left(\frac{Z_Y}{Z_K} \right) \text{ dB} \quad (9)$$

4. PRACTICAL EXAMPLE WITH A REAL MAGI³C POWER MODULE

To illustrate the rule of thumb, a sample calculation is carried out step by step based on the interference voltage result of an SIP-4 Power Module.

The electrical characteristics are: $V_{IN} = 12 \text{ V}$, $V_{OUT} = 5 \text{ V}$, $I_{OT} = 200 \text{ mA}$ (Order Code: **177920521**).

Figure 11 shows the result of the interference voltage measurement.

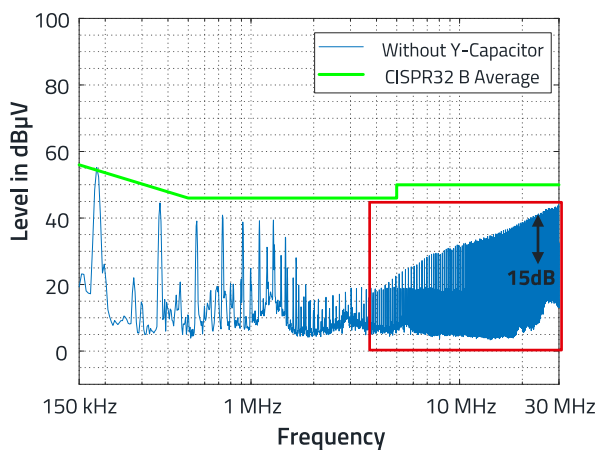


Figure 11: Interference voltage protocol, SIP-4 power module.

The calculation is based on a current clamp measurement; the frequency range considered here for the common mode interference is between 4 MHz and 30 MHz. In the frequency range below 4 MHz, the interference voltage is determined by the differential mode interference. Figure 11 shows that in the frequency range around 30 MHz, the distance of the interference voltage to the limit value according to CISPR 32 is approx. 12 dBμV.

The further design is based on an attenuation of 15dB in the 20 to 30MHz range, see Figure 11.

Step 1:

Determination of the desired attenuation in the frequency range from 4 MHz to 30 MHz.

Step 2:

Determine the coupling capacitance between the windings of the Power Module's transformer. The value for the coupling capacitance between the windings can be found in the data sheet of the power module. The value is usually specified as a maximum value, i.e. as a worst-case value. For the SIP-4 power module, 75 pF is specified for C_{ISO}, i.e. for C_K.

The value for C_{ISO} is typically determined at a measurement frequency of 100 kHz. For our calculation, however, C_K can be regarded as stable up to 30 MHz.

Step 3:

Calculation of the value for the bridge capacitor, based on the simplified equation.

$$A = \frac{Z_Y}{Z_K} \quad (10)$$

Conversion from the required attenuation of 15 dBV logarithmic to a linear value.

$$A = 10^{\left(\frac{x \text{ dB}}{20}\right)} = 10^{\left(\frac{-15 \text{ dB}}{20}\right)} = 0.177 \quad (11)$$

This results in a bridge capacitor value of:

$$C_Y = \frac{C_K}{d} = \frac{75 \text{ pF}}{0.177} = 421 \text{ pF} \approx 470 \text{ pF} \quad (12)$$

The value $C_Y = 470 \text{ pF}$ was chosen because it corresponds to a discrete component value.

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Step 4:

Verification of the value for the bridge capacitor using a real conducted EMC measurement, the result is shown in Figure 12.

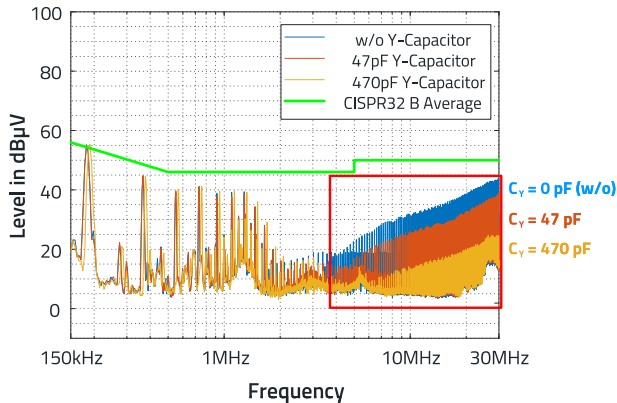


Figure 12: Measurement of conducted interference voltage with various bridge capacitors.

The greater the capacitance of the bridge capacitor, the higher the resulting attenuation in the frequency range above 3 MHz, as the path for the interference current has a lower impedance. It can also be seen that the attenuation with the real capacitance is higher than the calculated value. The calculation resulted in an attenuation of 17.2 dB for a bridge capacitor with a capacitance of 470 pF. However, the measurement shows an attenuation of almost 19 dB. This is a difference of 2 dB, which is due to the parasitic coupling capacitance C_K of the transformer, which changes the actual attenuation. The data sheet only specifies a maximum value. In practice, however, the coupling capacitance between the windings of the transformer is less than 75 pF, it is only 60 pF.

However, the deviation between the calculated and measured value can also be due to the measurement uncertainty, simplifications in the model and component tolerances.

5. LIMITS OF THE RULE OF THUMB & CONCLUSION

The bridge capacitor acts as a low-impedance bypass and minimises the interference current to the network simulation (LISN). However, due to its properties as a frequency-dependent impedance, the capacitor cannot 'keep out' the interference current over the entire frequency spectrum of the measuring range of the conducted interference voltage. The counterpart to the bridge capacitor is the coupling capacitance C_P to the environment. It is significantly influenced by the distance between the structure and the earth plate, but also by the length of the output lines. The bridge capacitor can only effectively divert the interference current if its capacitance is much greater than that of the coupling capacitance to the environment.

5.1 Validity of the simplification

The limits of the simplification are explained using a numerical example. The following values are selected for the variables involved in the example:

Parasitic coupling capacity to the environment C_P :

$$C_P = 20 \text{ pF} \rightarrow Z_P = 795 \Omega @ 10 \text{ MHz.}$$

Bridging capacitor C_Y :

$$C_Y = 470 \text{ pF} \rightarrow Z_Y = 34 \Omega @ 10 \text{ MHz}$$

Parasitic winding capacitance C_K :

$$C_K = 75 \text{ pF} \rightarrow Z_K = 212 \Omega @ 10 \text{ MHz}$$

Impedance of LISN Z_V :

$$Z_V = 25 \Omega$$

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The equation for the required attenuation α then becomes:

$$A = \frac{Z_Y \cdot (Z_K + Z_P + Z_V)}{(Z_K + Z_Y \parallel (Z_V + Z_P)) \cdot (Z_V + Z_P)} \quad (13)$$

$$A = \frac{Z_K + Z_P + Z_V}{Z_K + Z_P + Z_V + \frac{Z_K}{Z_Y} \cdot (Z_P + Z_V)} \quad (14)$$

$$A = \frac{212 \, \Omega + 795 \, \Omega + 25 \, \Omega}{212 \, \Omega + 795 \, \Omega + 25 \, \Omega + \frac{212 \, \Omega}{34 \, \Omega} \cdot (795 \, \Omega + 25 \, \Omega)} \quad (15)$$

$$A = \frac{1032 \, \Omega}{1032 \, \Omega + \frac{212 \, \Omega}{34 \, \Omega} \cdot 820 \, \Omega}$$

$$A = 0.1679 = 0.168$$

It is noticeable in the equation that the numerator and denominator values are close to each other. These are marked in red to make them easier to read.

$$A = \frac{1032 \, \Omega}{1032 \, \Omega + \frac{212 \, \Omega}{34 \, \Omega} \cdot 820 \, \Omega} \quad (16)$$

The values marked in red are all approx. 1000. If we now replace the values with 1000, the equation can be simplified as follows.

$$\alpha = \frac{1000 \, \Omega}{\left(1 + \frac{212 \, \Omega}{34 \, \Omega}\right) \cdot 1000 \, \Omega} \quad (17)$$

The 1 in the bracket in the denominator can be deleted as it is more than 6 times lower than $212 \, \Omega / 34 \, \Omega$

$$A \approx \frac{34 \, \Omega}{212 \, \Omega} \approx 0.16 \quad (18)$$

If the results of the two variants of the formula are compared, the following difference emerges: see Table 2.

The following illustration (Figure 13) serves to better assess this effect or situation:

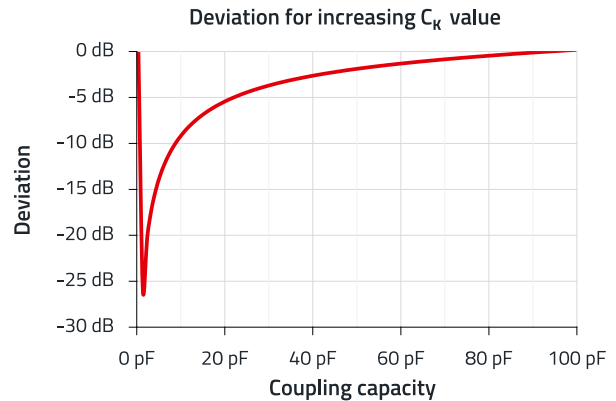


Figure 13: A Deviation as a function of the parasitic coupling capacitance C_P and the parasitic winding capacitance C_K .

The graph clearly shows that the error in applying the 'short formula' increases the closer the coupling capacitance C_K of the transformer is to the determined value of the parasitic coupling capacitance C_P .

5.2 Conclusion

The great effect of a bridge capacitor in reducing the common mode interference voltage was proven by measurement. The measurements have also clearly shown that the theoretical approach using the formula determined is a good way to determine a starting value for a bridge capacitor. The formula can always be used in its long form as it has no simplification based on the ratios between C_P and C_K . Only when using the short formula must attention be paid to the ratio between C_P and C_K as it has an essential influence on the effectiveness of the formula.

Variant long formula	Variant short formula
$a = 20 \cdot \text{Log}(0.168) = -15.49 \, \text{dB}$	$a = 20 \cdot \text{Log}(0.16) = -15.91 \, \text{dB}$
$\Delta a = -0.42 \, \text{dB}$	

Table 2: Comparison of both variants of the formula.

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REVISION HISTORY

Document Version	Release Date	Changes
ANS022a	2025/04/16	Initial release of the application note

Note: The current version of the document and the release date are indicated in the footer of each page of this document.