APPLICATION NOTE

ANO009 | Understanding parameters in ICLED datasheets

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INTRODUCTION TO ICLED

ICLEDs, also referred to as addressable LEDs or smart LEDs, are light-emitting diodes (LEDs) that incorporate an integrated circuit (IC) within their design (as seen on Figure 1). This device, by means of pulse width modulation (PWM), enables individual control of the red, green, and blue chips in the package. Thus, granting fine and precise control for color mixing solutions.
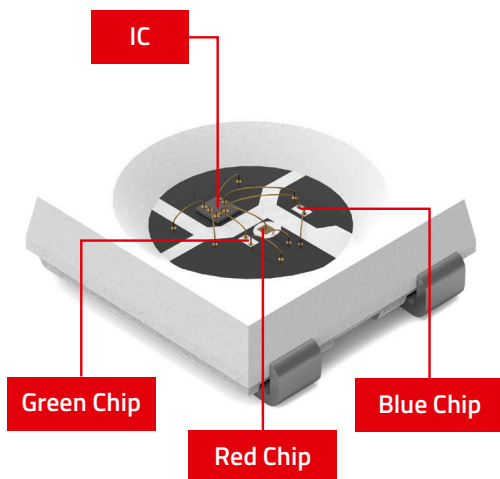

Figure 1: Illustration of the internal components of an ICLED (WE PN: 1315050930002)

The datasheet of an ICLED describes and summarizes the performance and technical characteristics of the products. As the ICLED differs from an "analog" LED, a new datasheet from Würth Elektronik with drawing specifications and performance graphs is introduced into the market. In addition to the information stated in the datasheet, Würth Elektronik provides this application note as a guideline on how to effectively read an ICLED datasheet from WE.

Figure 2 introduces the first page of an ICLED datasheet (PN: 13150509030002). An overview of the order code, release date, drawing tolerances (norm) and the certifications of the product can always be found at the bottom center of each page of the data sheet.
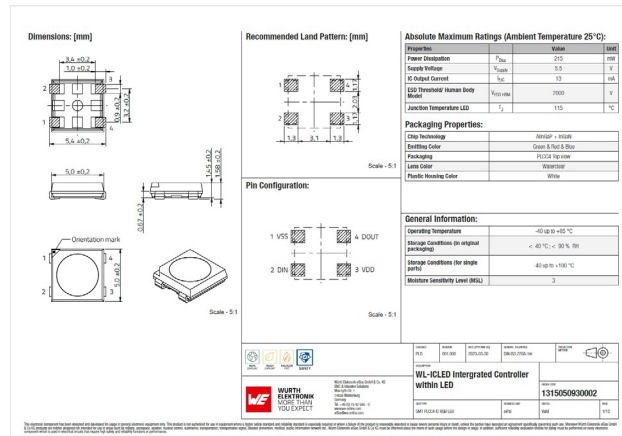

Figure 2: First page of the 1315050930002 ICLED

The general structure of the ICLED datasheets is explained below:

Dimensions, recommended land pattern and pin configuration

The first section (*Dimensions: [mm])* introduces a technical drawing of the selected PN. As the LEDs have different sizes and number of connections (pins), WE introduces the *Recommended Land Pattern* as a reference to create the footprint of the selected component in any PCB design software (e.g., Altium or Eagle). Regarding the stencil's thickness, Würth Elektronik recommends a value of 120 μm. The pin configuration depicts the name of the pins corresponding to the soldering position of the ICLED (top view). An example of the presented drawing is shown on Figure 3.

The ICLED requires both power supply and communication pins, therefore the naming of the pins is defined as:

V_{DD}: This pin is used to supply power to the ICLED component (typ. +5 V).

V_{SS}: The pin is connected to the ground or common reference of the power supply. It serves as the return path for the current flowing through the ICLED.

1. D_{IN} (Data Input): This pin is responsible for receiving data signals that control the color and intensity of the ICLED. The data signal usually consists of a series of digital bits (1 or 0) encoded as a combination of logical levels (high and low) to specify the intensity values of the RGB LEDs within the package.

2. D_{OUT} (Data Output): This pin is responsible for the transmission of the digital data to next ICLED connected in the circuit. The data output from one ICLED is connected to the D_{IN} pin of the next ICLED (daisy chain connection).

Figure 3: Dimensions (left), recommended land pattern (top right) and pin configuration (bottom left) of 1315050930002 ICLED

Absolute maximum ratings

The table depicted in Figure 4 indicates the absolute maximum ratings (input and output) of the ICLED to ensure proper usage, prevent damage, and maximize the lifespan of the component.

Please note that the *IC Output Current* (I_{F},I_{C}) represents the current delivered from the IC to each individual R, G, B chip, this value is tested during the IC production process. However, as the IC itself is an active component, it requires energy to function properly. Nonetheless, the customer receives an enclosed package (IC with LED chips) these values cannot be measured individually. For this reason, the current to be measured on an ICLED consists of the operating current of the IC ($I_{DD, ON}$) in addition to the IC output current. ($I_{F, IC}$), as depicted in Figure 5.

As previously mentioned, the value of the driving current is defined for one LED. In view of this, the maximum power dissipation is calculated by considering the total. current consumption of the LED. As the ICLED includes three chips, the total current consumption is tripled (the operating current of the IC ~1 mA is already included in the calculation).

The maximum power dissipation of the LED is calculated as indicated by Equation (1):

$$P_{Diss} = I_{DD\,T} \cdot V_{DD\,Max} = (3 \cdot 14,5\ mA) \cdot 5,5\ V = 239,25\ mW \cong 240\ mW \tag{1}$$

Equation 1: Calculation of the total power dissipation of an ICLED

Properties		Value	Unit
Power Dissipation	P_{Diss}	240	mW
Supply Voltage	V_{Supply}	5.5	V
IC Output Current	$I_{F,IC}$	14.5	mA
ESD Threshold/ Human Body Model	$V_{ESD\,HBM}$	4000	V
Junction Temperature LED	T_J	115	°C

Figure 4: Absolute maximum ratings (PN: 1315050930002)

Figure 5: Differences on the IC Output current (orange), IC operating current (cyan) and total current of an ICLED (magenta)

Packaging properties

This section covers the physical characteristics and specifications of the package in which the IC and LED chips are encapsulated. Information such as LED-chip technology, packaging specifications (PLCC or Chip LED), color of the packaging (only for PLCC ICLEDs) as well as the lens type (waterclear or diffused) can be found in the table shown in Figure 6. Note that independent of the LED model, the

emitting color field refers to the order in which the LEDs light up in the communication protocol (e.g. GRB, RGB, BGR, etc.).

Chip Technology	AlInGaP + InGaN
Emitting Color	Green & Red & Blue
Packaging	PLCC4 Top view
Lens Color	Waterclear
Plastic Housing Color	White

Figure 6: Packaging properties table

General information

From the information on the table below (Figure 7) the ambient conditions for operation and storage of ICLEDs is shown. Typically, the ICLEDs of WE operate at ambient temperature between -40°C and +85°C, in case operating temperature is outside the defined range it can lead to a reduced lifetime or even to complete failure of the component. Note that the Moisture Sensitivity Level (MSL) can be found at the end of the mentioned table. ICLEDs from WE are classified as MSL 3[1], meaning at least 168 hours of floor life after the original packaging has been opened.

Operating Temperature	-40 up to +85 °C
Storage Conditions (in original packaging)	< 40 °C ; < 90 % RH
Storage Conditions (for single parts)	-40 up to +100 °C
Moisture Sensitivity Level (MSL)	3

Figure 7: General information table

Optical properties

The characteristics related to light emission of the individual R, G, B chips are presented on the table in Figure 8. The test conditions described next to the parameters indicate the voltage level (V_{DD}) and the digital signal sent from the test microcontroller to the D_{IN} pin of the ICLED. The capacitor (C) is included in the measurement process to prevent voltage drops and minimizing current spikes during the PWM control of the IC.

Properties		Test conditions	Value min.	Value typ.	Unit
Peak Wavelength (Red)	$\lambda_{Peak\ R}$	VDD = 5V, VSS = 0V Bit Code: 0x00FF00 C = 100nF		630	nm
Peak Wavelength (Green)	$\lambda_{Peak\ G}$	VDD = 5V, VSS = 0V Bit Code: 0xFF0000 C = 100nF		520	nm
Peak Wavelength (Blue)	$\lambda_{Peak\ B}$	VDD = 5V, VSS = 0V Bit Code: 0x0000FF C = 100nF		465	nm
Dominant Wavelength (Red)	$\lambda_{Dom\ R}$	VDD = 5V, VSS = 0V Bit Code: 0x00FF00 C = 100nF		625	nm
Dominant Wavelength (Green)	$\lambda_{Dom\ G}$	VDD = 5V, VSS = 0V Bit Code: 0xFF0000 C = 100nF		525	nm
Dominant Wavelength (Blue)	$\lambda_{Dom\ B}$	VDD = 5V, VSS = 0V Bit Code: 0x0000FF C = 100nF		470	nm
Luminous Intensity (Red)	$I_{V\ R}$	VDD = 5V, VSS = 0V Bit Code: 0x00FF00 C = 100nF	280	450	mcd
Luminous Intensity (Green)	$I_{V\ G}$	VDD = 5V, VSS = 0V Bit Code: 0xFF0000 C = 100nF	900	1300	mcd
Luminous Intensity (Blue)	$I_{V\ B}$	VDD = 5V, VSS = 0V Bit Code: 0x0000FF C = 100nF	150	260	mcd
Spectral Bandwidth (Red)	$\Delta\lambda\ R$	VDD = 5V, VSS = 0V Bit Code: 0x00FF00 C = 100nF		14	nm
Spectral Bandwidth (Green)	$\Delta\lambda\ G$	VDD = 5V, VSS = 0V Bit Code: 0xFF0000 C = 100nF		28	nm
Spectral Bandwidth (Blue)	$\Delta\lambda\ B$	VDD = 5V, VSS = 0V Bit Code: 0x0000FF C = 100nF		18	nm
Viewing Angle Phi 0°	$2\theta_{50\%}$			120	°

Figure 8: Optical Properties table

Electrical properties

The electrical properties table from Figure 9 define the operating boundaries of the ICLED. From the information on table, the operating supply voltage of the ICLED V_{DD} is defined (typ. between 3.5 V and 5.5 V).

Properties		Value min.	Value typ.	Value max.	Unit
Operating supply voltage	V_{DD}	3.5	5	5.5	V
Digital input voltage - high-level	V_{IH}	0.7 * VDD		VDD	
Digital input voltage - low-level	V_{IL}			0.3 * VDD	
Digital output voltage - high-level	V_{OH}	0.9 * VDD			
Digital output voltage - low-level	V_{OL}			0.1 * VDD	
IC Output Current	I_{FIC}		13	14.5	mA
IC Standby Current	$I_{DD,OFF}$			1	mA

Figure 9: Electrical properties table

V_{IH} and V_{IL} specify the electrical requirements of the signal received through the D_{IN} pin of the ICLED. Any input voltage greater than V_{IH} is guaranteed to be recognized as a logic high state while any input voltage lower than V_{IL} is guaranteed to be recognized as a logic low state. Typically, V_{IH} and V_{IL} are defined as a percentage of the operating supply voltage (V_{DD}). According to the values of the table in Figure 9 and assuming an operating voltage of V_{DD} = 5 V, can obtain the values for V_{IHmin} and V_{ILmax} as indicated in Equation (2) and (3):

$$V_{IH_{min}} = 0.7 * V_{DD} = 3.5\ V \qquad (2)$$

Equation (2): Calculation of V_{IHmin} for V_{DD} = 5V

$$V_{ILmax} = 0.3 * V_{DD} = 1.5\ V \qquad (3)$$

Equation (3): Calculation of V_{ILmax} for $V_{DD} = 5\ V$.

In case the supply voltage of the ICLED is not 5 V, the values for V_{IH} and V_{IL} should be calculated as explained before. V_{OH} and V_{OL}, on the other hand, refer to the voltage levels that determine the output levels of the signal transmitted from the D_{OUT} pin of the ICLED. It is expected that the voltage level of a high logic state to be over V_{OH} and when outputting a low logic level, the voltage value is lower than V_{OH}. This ensures that the voltage levels of the output signal to be recognized by the subsequent ICLED connected in the circuit. The Figure 10 depicts a graphical representation of the voltage values that define the operation range of the ICLED.
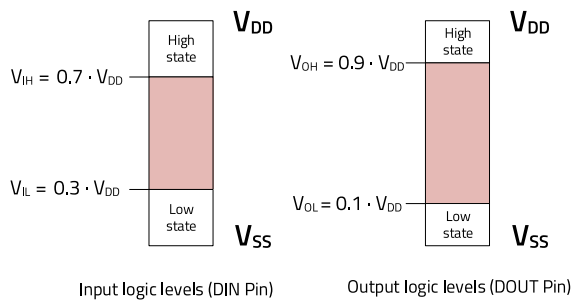
Figure 10: Graphical representation of the electrical operating boundaries of an ICLED

$I_{F,IC}$ describes the driven current from the IC to the individual LED chips and $I_{DD, OFF}$ corresponds to the operating current of the IC when all LED chips are turned off (PWM level of each chip equal to 0b0000000 or 0x00000) – also known as standby current.

Schematic of the ICLED

Würth Elektronik introduces an ICLED schematic depicted in Figure 11. This schematic depicts the internal connections between the IC and the LEDs chips and the order of appearance of the LED chips (from left to right) corresponds to the order in which these light up according to the communication protocol. In other words, there is no standard layout of the LED chips and depending on the manufacturer, the order of appearance changes (e.g., GRB as in the picture below, RGB, BGR, RBG, etc.)
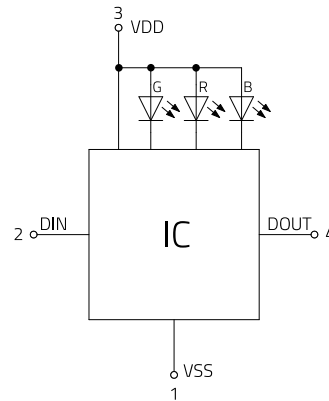
Figure 11: Schematic of an ICLED

Switching characteristics

The switching characteristics define the response time of the ICLED regarding the characteristics of the PWM signal, as well as the propagation delay of the output signal (with respect to the input signal). The parameters depicted on Figure 12 are briefly explained below: Assuming the following electrical operating values of an ICLED:

$$V_{DD} = 5V;\ V_{IH} = V_{OH} = V_{DD} \qquad (4)$$

and

$$V_{IL} = V_{OL} = 0V \qquad (5)$$

1. tPLH [s]: Propagation delay where the input signal (D_{IN}) crosses 50% of V_{DD} to where the output signal (D_{OUT}) crosses 50% of V_{DD} when switching from low to high level.
2. tPHL [s]: Propagation delay where the input signal (D_{IN}) crosses 50% of V_{DD} to where the output signal (D_{OUT}) crosses 50% of V_{DD} when switching from high to low level.
3. tR [s]: Time interval of the rising edge of the PWM pulse (to one LED chip) from 10% to 90% of the pulse's amplitude (V_{LED} or $V_{OUT\ RGB}$).
4. tR [s]: Time interval of the falling edge of the PWM pulse (to one LED chip) from 10% to 90% of the pulse's amplitude (V_{LED} or $V_{OUT\ RGB}$).
5. fPWM [Hz]: Frequency of the PWM signal that controls the single R, G, B chips.
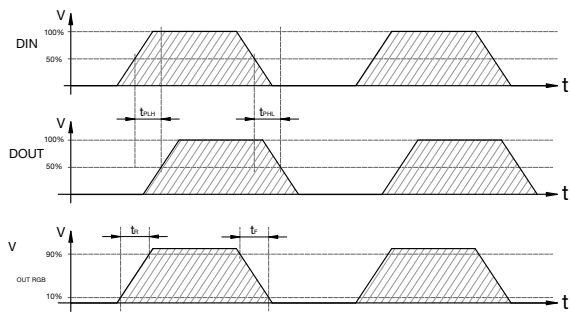
Properties	Symbol	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Frequency of the PWM	fPWM			2.5		kHz
Transmission Delay Low to High	tPLH	DIN to DOUT		150		ns
Transmission Delay High to Low	tPHL	DIN to DOUT		150		ns
Rise Time	tR			50		ns
Fall Time	tF			50		ns

Figure 12: Input and output waveforms of an ICLED. Table indicates the typ. timing of the expected signals.

Data transfer time

The single wire communication protocol is formed by 24-bit data for each R, G, B LED. The data is formed by red, green, and blue data (not necessarily in this order), each with 8-bit width, and transferred with most significant bit (MSB) first. In case that two or more ICLED are daisy chained, the IC receives the first 24 bits of information and retransmits the remaining n-bits through the D_{OUT} pin into the next ICLED. Each bit is recognized by a combination of both a high and a low logic pulse received through the D_{IN} pin; the timing of these pulses defines if the IC recognizes the signal as a logical 1 or a logical 0. The logical bit 0 is represented by a pulse of length T0H with a high voltage level ≥ V_{IH} and a pulse of length T0L with low voltage level ≤ V_{IL}. Whereas a logical bit 1 is represented by a T1H with a high voltage level ≥ V_{IH} and a pulse of length T1L with low voltage level ≤ V_{IL}. In order for the ICLED to receive a new information package, a low pulse longer than T_{reset} is required.

The table depicted in the Figure 13 defines the timing required by the single wire communication protocol of the IC to distinguish between a logical bit 1, a logical bit 0 or a reset pulse.

Properties	Symbol	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Bit Period	T			1250		ns
Bit 0 High Pulse	T0H		320	350	400	ns
Bit 0 Low Pulse	T0L		800	900		ns
Bit 1 High Pulse	T1H		640	750	800	ns
Bit 1 Low Pulse	T1L		350	400		ns
Reset Pulse	Treset		200			□s

Figure 13: Data transfer timetable

Sequence chart

The Figure 14 provides a graphical representation of the single wire communication protocol. On the top part, the composition of the 24-bit data is depicted (e.g., GRB). As information of this communication protocol is sent with Most Significant Bit (MSB) first the data is transmitted from the leftmost bit (e.g., G7) moving towards the rightmost bit of each color data (G6, G5, G4... until G0). For illustration purposes, G7 and G6 are rewritten as 1 and 0 for the user of this datasheet to have a visual representation of the parameters that define the logical bit 1 and the logical bit 0 respectively. The graph on the bottom side of the figure represents the reset code (not to scale with the graphs for Bit 1 or Bit 0)
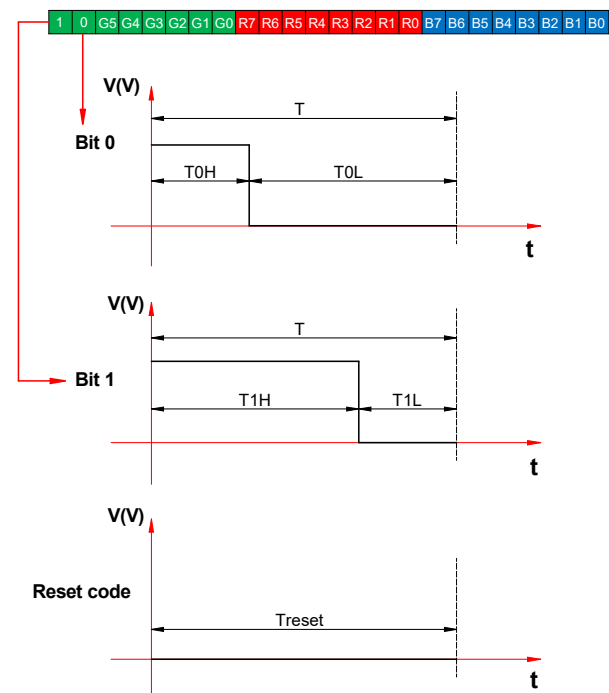
Figure 14: Graphical representation of the single wire communication protocol and the chip layout of an ICLED

Data transmission method

As the ICLEDs are designed to be daisy chained (by connecting the D_{OUT} pin of one LED to the D_{IN} pin of the next LED), Figure 15 illustrates the transmission of the information between an "N" number of ICLEDs
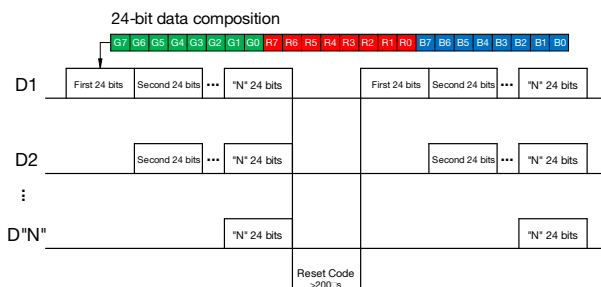
Figure 15: Representation of the data transmission method of SW ICLEDs

Define D1 as the information package sent from an MCU to the first ICLED, D2 is then the information package transmitted at the output of the first ICLED. D"N" is therefore the digital information transmitted at the output of the "N-1" ICLED in the chain. The figure illustrates that each time an ICLED receives a data package, the IC will reduce the information by 24 bits and retransmits the remaining ones into the next LED in the chain. A reset code should be read by the D_{IN} pin of the first ICLED to indicate that a new information package is going to be transmitted.

Typical application circuit

The typical application circuit of an ICLED system is presented in the Figure 16, with the microcontroller (MCU) as the component that generates the data signals. This data signal is connected from the MCU to the D_{IN} pin of the first ICLED, the rest components are then daisy chained.
Würth Elektronik recommends the ICLEDs to be connected at V_{DD} = +5 V and the addition of a bypass capacitor (C ~ 100 nF) as close as possible to the V_{DD} pin of each ICLED to ensure a stable power and to block voltage fluctuations caused by the switch-on and switch-off currents of the ICLEDs. It is important to mention that this application circuit design may vary depending on the individual specifications/requirements from the customer's application.
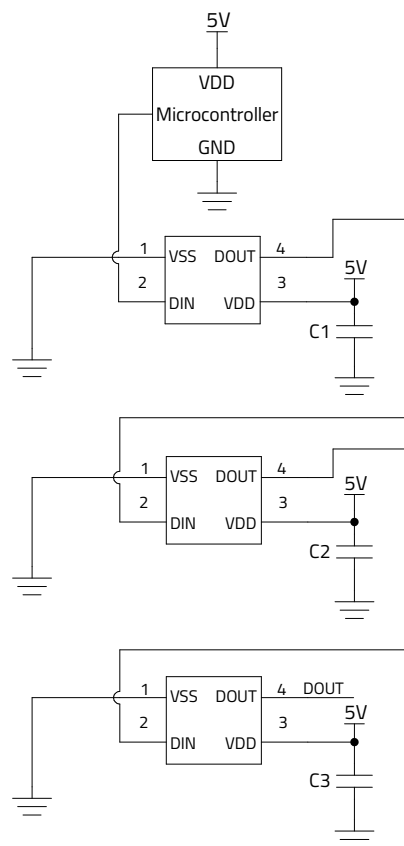
Figure 16: Typical application circuit of SW ICLEDs

Typical radiation plots of an ICLED

As a standard for WE, the graph presented in Figure 17 denotes the radiation pattern of an LED in both cardinal (left side) and polar coordinates (right side). The viewing angle of the LED is indicated by the FWHM angle or, in other words, where the intensity of the LED drops by 50%. For the 1315050930002 the viewing angle is then 120° (e.g., a Lambertian radiator).
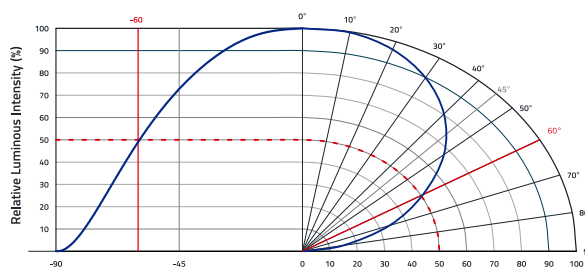
Figure 17: Viewing angle of an ICLED.

The graph in Figure 18 provides the normalized emission spectrums of the single red, green and blue LED chips inside the ICLED (measured at PWM equal to 100%)
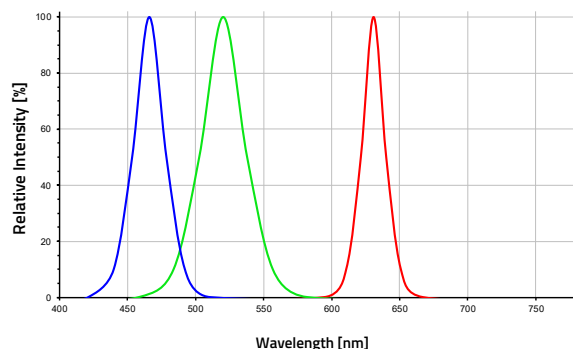
Figure 18: Spectral characteristics of the R, G, B LEDs inside the ICLED

Typical luminous intensity vs. Bit Code

Figure 19: Dynamic plot luminous intensity (in mcd) vs 8-bit digital signal (for each color)

Luminous intensity vs bit-code

As already mentioned, the R, G, B LED chips are controlled via PWM signal at a fixed current level. For this reason, the 256 brightness (8-bit) internal for each LED was subdivided and the luminous intensity values were performed at these selected subdivisions. The Figure 19 plots the typical luminous intensity of the single R, G, B LEDs against the 8-bit brightness selector of the corresponding color.

Packaging specification

The packaging specification consists of a detailed drawing of the tape and reel in which the LEDs can be ordered as indicated on Figure 20.
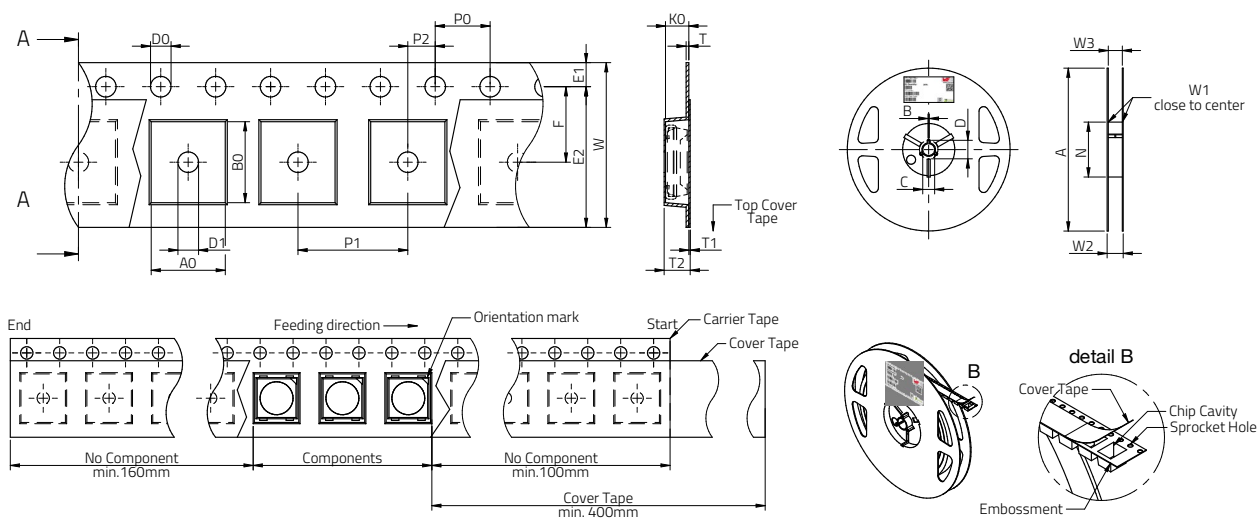
Figure 20: Tape and Reel-Specifications

A.1 References

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