Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

RD006 // Eleazar Falco

1 Overview

This reference design presents an auxiliary supply with two output voltage rails of 5 V, galvanically-isolated from each other, with a combined maximum output power of up to 3 W (i.e. 0.3 A output current per rail). Tightly regulated, lower voltage rails like 3.3 V, 2.5 V or 1.2 V can be easily obtained by cascading a low-dropout linear voltage regulator (a.k.a. LDO) to the required output rail. The design targets applications like isolated communication interfaces and data acquisition systems, as well as many systems using sensors, voltage-level-shifters, digital isolators, or opto-couplers, amongst others.

Key Features

- Extremely compact (20 x 20 x 5.3) (L x W x H) (mm)
- Wide input voltage range from 18 to 32 V
- Primary output voltage: 5.1 V ± 1%
- Secondary output voltage (balanced load): 4.8 V ± 5%
- Secondary output voltage (unbalanced load): 4.8 V ± 10%
- Output power up to 3 W
- Peak efficiency of 82 %
- LM25017 IC Controller (Texas Instruments)
- WE-TDC-HV Coupled Inductor with 2 kV Isolation
- Buck converter with additional isolated output topology

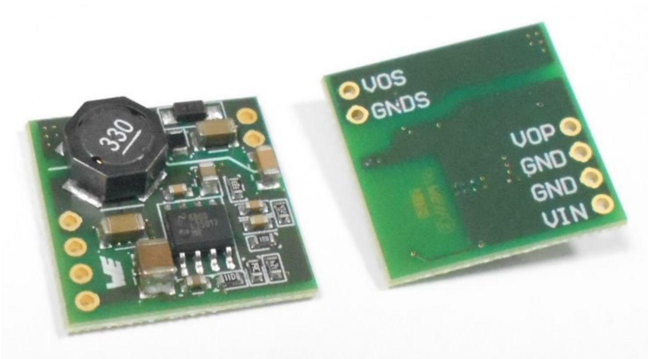

Figure 1: Board Image (top and bottom sides)

Typical Applications

- Programmable Logic Controllers (PLC)
- Distributed Control Systems (DCS)
- Data Acquisition Systems (DAQ)
- Isolated Signal and Communication Interfaces
- Voltage level shifting
- Sensor and actuator systems

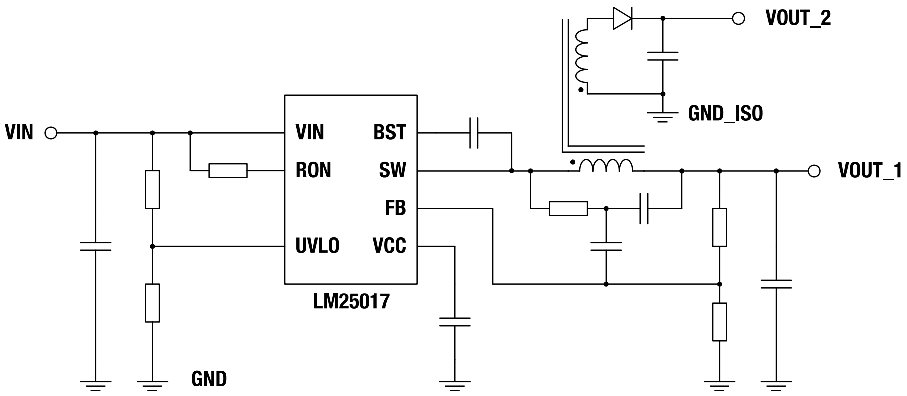

Figure 2: Simplified schematic

2 Technology and System Design Considerations

Some applications require two low-power bias voltage supply rails, of the same or different value, and with one of these rails being galvanically isolated from the other. This isolated output can be easily obtained from a standard synchronous buck converter. This is accomplished by replacing the single power inductor with a coupled-inductor, and adding a diode-capacitor peak rectifier circuit (Flyback-like) to the available secondary winding (Figure 3). This topology is named as Flybuck™by Texas Instruments and as Iso-buck™by Maxim Integrated.

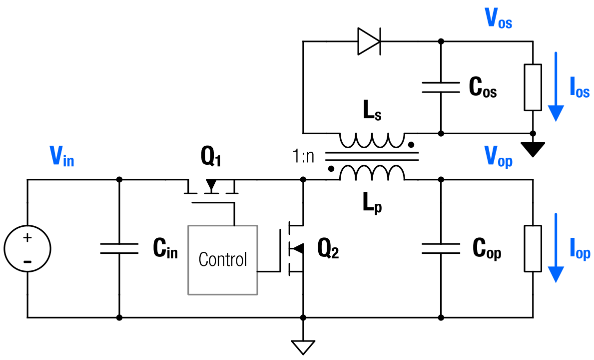

Figure 3: Buck Converter with Isolated Output Power Stage

The topology takes advantage of the fact that the well-regulated output voltage of the buck converter appears across the primary winding of the coupled inductor during the off-time window of the control MOSFET (Q_1). This voltage is reflected to the secondary winding, scaled by the secondary-to-primary turns-ratio (n), and with the diode forward-biased, it would appear directly at the output of the isolated rail. During the on-time of Q_1, the rectifier diode is reverse-biased and the output capacitor supplies the isolated load. Note the winding dot arrangement and thus polarity between the primary and secondary winding required to achieve this functionality. The isolated output voltage is therefore only ‘indirectly’ regulated, as it ‘tracks’ the primary output voltage. In the case with ideal components, it would be obtained:

$$V_{os} \approx n \cdot V_{op}$$

2.1 Isolated Output Regulation

The final voltage obtained on the isolated output V_{os} will be affected by several parameters, not only by the primary and secondary load currents and forward voltage drop across the diode, but also by operating conditions like the duty cycle and switching frequency, as well as component parasitic elements like Q_2 ON-resistance(R_{ds}), primary and secondary winding resistances (R_p. R_s) as well as the leakage inductance of the coupled-inductor (L_k). Figure 4 shows the equivalent circuit during the off-time window of Q_1.

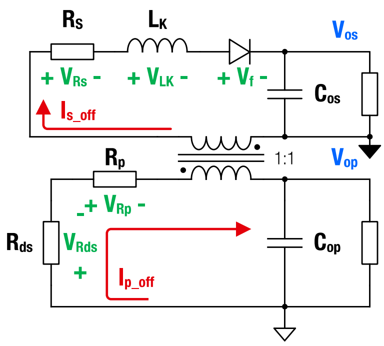

Figure 4: Equivalent circuit with parasitic elements during OFF-time of Q_1 (open)

The average voltage drops across the parasitic elements on the primary and the secondary sides during this off-time window will determine the final voltage level of the isolated output, as follows:

$$V_{os} \approx V_{op} + V_{Rds} + V_{Rp} - V_f - V_{Lk} - V_{Rs}$$

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

These voltage drops depend on the average currents through the primary and secondary winding during the off-time which, in turn, directly depend on the output load currents.

In good designs, the isolated output load regulation can be found typically in the range of 5 to 15%. Such tolerance is still acceptable in many applications using ICs which accept a wide bias supply range, like digital isolators, serializer/deserializers, communication transceivers, etc.

For further information, a detailed analysis of the converter operation and important design considerations of this topology, please refer to the application note ANP017.

2.2 Obtaining tightly-regulated isolated bias voltages

For applications requiring different and/or very tightly regulated bias supply voltages, such as precision analog-to-digital converters (ADCs) or precision amplifiers in input/output analog PLC modules, low-dropout linear voltage regulators (a.k.a. LDOs) can be added to the output rails. When doing so, in order to ensure tight regulation over the full load current range, it is very important that at the maximum load current and worst-case conditions, the isolated output voltage (V_{os}) stays higher than the minimum dropout voltage value of the LDO given in its datasheet (V_{LDO_min}) plus the set output voltage (V_{os_reg}):

$$V_{os} > V_{LDO\_min} + V_{os\_reg}$$

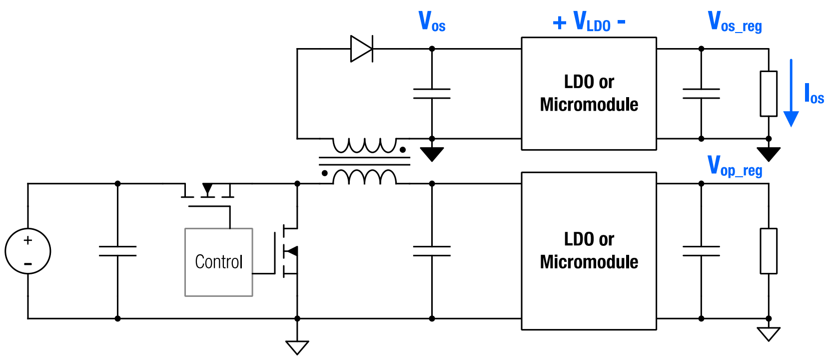

Figure 5: Adding LDOs or DC-DC Micromodules for tightly-regulated output voltage rails and different voltage supplies

LDOs are 'pass-transistors' and can be effectively modelled as a variable resistor. The power dissipated in the LDO of the isolated rail above would be:

$$P_{LDO} = (V_{os} - V_{os\_reg}) \cdot I_{os}$$

As the current or dropout voltage increases, efficiency will drop as the power losses are higher and a larger copper thermal heatsink area will be required on the PCB, increasing with it the overall solution size.

DC-DC micromodules like the Magi³C-VDMM series from Würth Elektronik are a high-performance alternative to LDOs, especially in cases where thermal performance and small overall solution size are paramount. Since they are, in fact, switching regulators, they operate at very high efficiency, being capable of sourcing higher currents with very low losses and thus a much smaller heatsink area is required.

2.3 Example PLC Analog Input Module System

Figure 6 below shows an example of using the RD006 in an analog input module, a common part of programmable logic controller devices widely used in industrial automation. The analog voltage levels received from the field sensors (e.g. ranges 0-10 VDC, 0-5 VDC) are multiplexed and fed to the programmable gain amplifier (PGA) and analog-to-digital converter (ADC) for the required precision signal conditioning and conversion. Depending on the devices used, they could be supplied directly by V_{os} or by a tightly regulated isolated voltage rail with an LDO (V_{os_r}). A multi-channel digital isolator provides galvanic isolation between the ADC in the field side and the controller, which typically communicate via SPI or I2C protocols. The primary output voltage V_{op} supplies the controller-side of the digital isolator and on-board MCU (an LDO can be again cascaded for 3.3 V devices). Note that this is an example system with devices requiring only unipolar voltage supply. Depending on the specific requirements, other system implementations may require bipolar supplies. Special ICs already integrating several of the system blocks, like the MUX, PGA and ADC, can also be found, with some even providing also the galvanic isolation. These are typically used in systems where compact size and high integration is paramount.

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

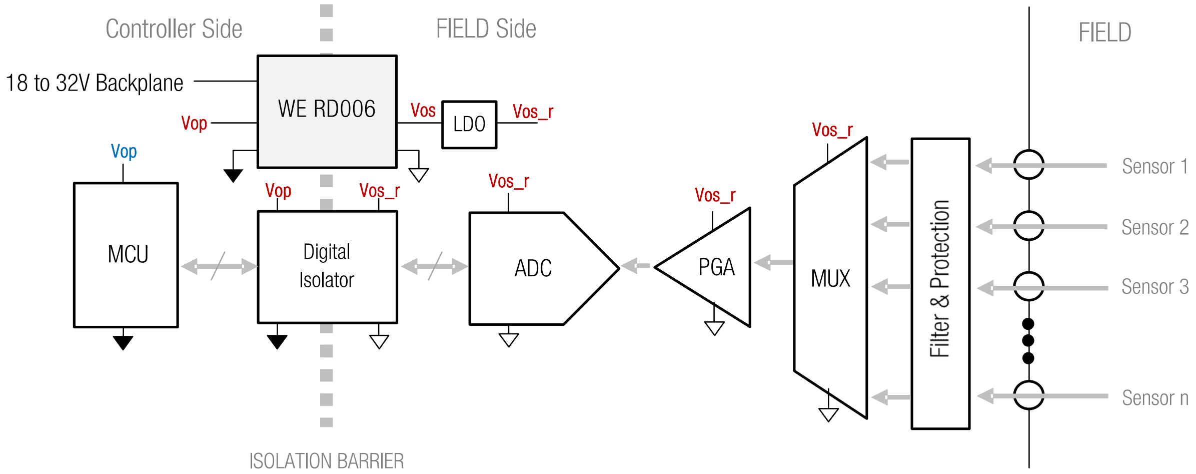

Figure 6: Multichannel PLC Analog Input Module example (simplified)

2.4 Example Isolated Communication Interface Transceiver System

Many systems communicating with several devices over large distances use RS-485 communication protocol. In such systems, isolation often becomes essential in order to prevent the adverse effects of ground loops, which worsen as the distance between the devices increases. Below an example of using the RD006 in an RS-485 isolated communication interface. For other communication protocols, similar systems are implemented.

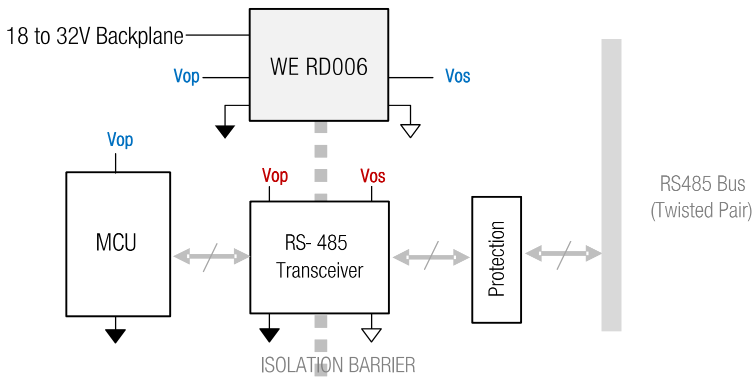

Figure 7: Isolated RS-485 transceiver system (simplified)

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

WÜRTH ELEKTRONIK

3 Electrical Specification

	Minimum	Nominal	Maximum	Units
Input Voltage (V_{in})	18	24	32	(V)
Primary Output Voltage (V_{op})	5.08	5.1	5.19	(V)
Secondary Output Voltage (V_{os_bal}) (@ balanced load) (*)	4.56		4.93	(V)
Secondary Output Voltage (V_{os_unb}) (@ unbalanced load) (**)	4.26		5.25	(V)
Primary Output Current (I_{op})	0		300	(mA)
Secondary Output Current (I_{os})	0		300	(mA)
Output Power (P)	0		3	(W)
Switching Frequency (F_{sw})		480		(kHz)

Table 1: Electrical specification table

NOTE: Specification at 25 °C ambient temperature

(*) balanced load means that the load current of the isolated output is the same (or nearly the same) as the load current of the non-isolated output

(**) unbalanced load means that the load current of the isolated output is different from the load current of the non-isolated output

4 Schematic

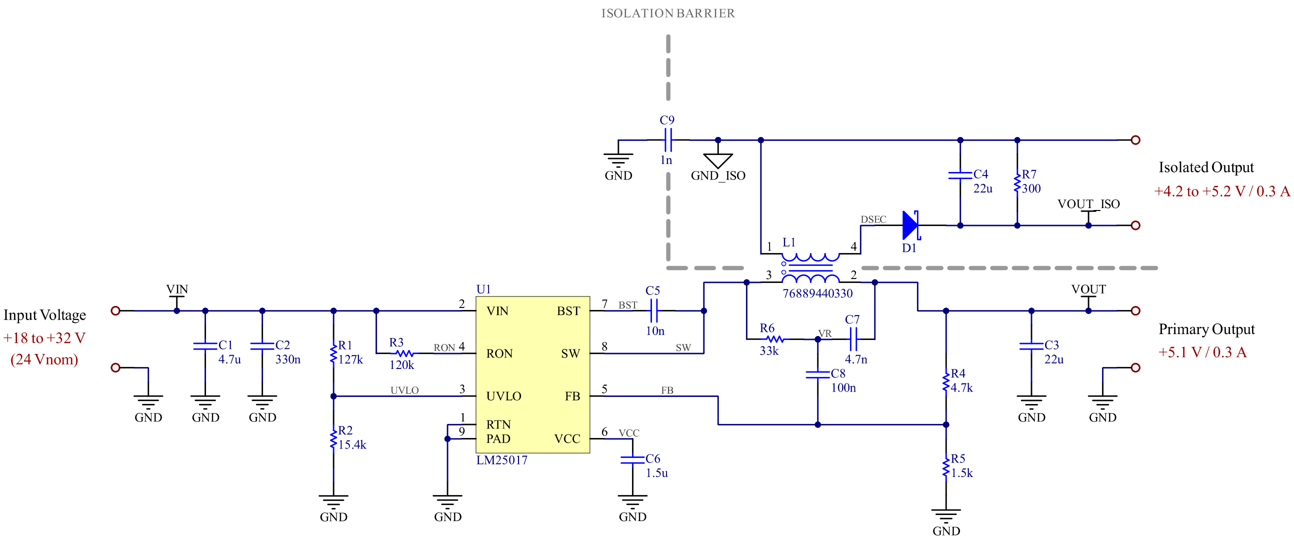

Figure 8: RD006 Schematic

5 Board layout and Dimensions

The design is a 2-layer PCB with components only on top side. The full SMT (surface-mount technology) components design enables pick and place assembly automation and lower manufacturing costs. Note that the PCB design can be integrated into a larger system PCB or alternatively used as a plug-in module by using straight pin or socket headers with 2.54 mm pitch from the WR-PHD series from Würth Elektronik (e.g. 61300411121 (4-pin) for non-isolated input and output and 61300211121 (2-pin) for isolated output). The PCB layout files (Altium Designer 21) as well as the PCB fabrication files are available to download on Würth Elektronik website and on this link: LINK.

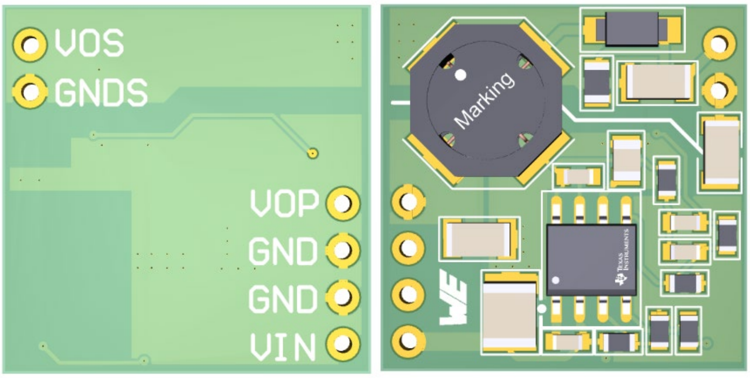

Figure 9: RD006 Board 3D detail: top side (left)(top view), bottom side (right)(bottom view)

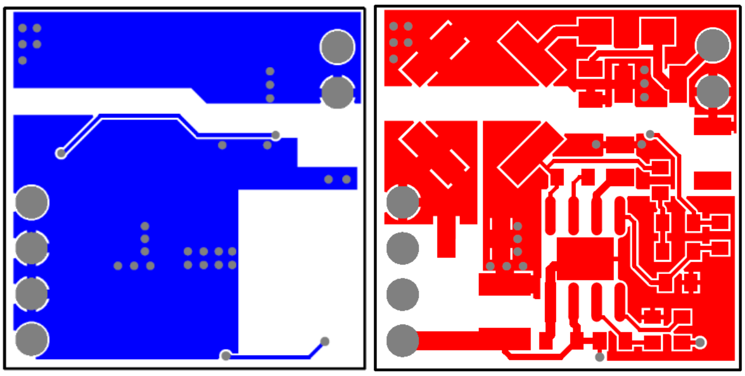

Figure 10: RD006 PCB Layout: top layer route (left), bottom layer route (right) (both top view)

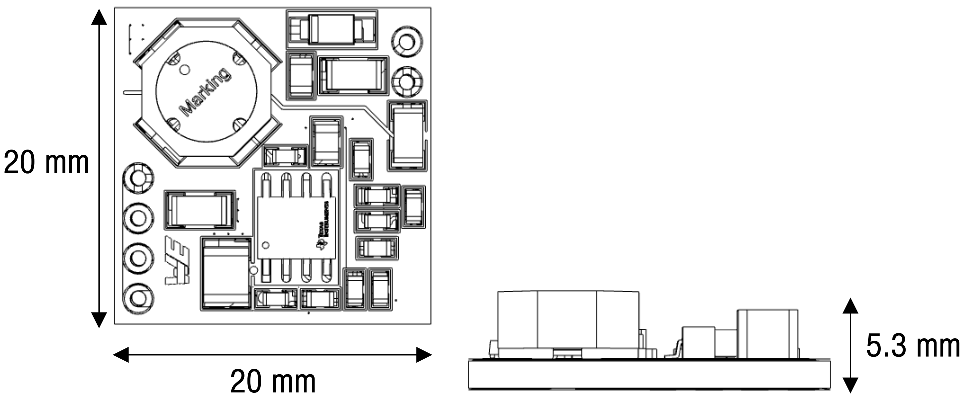

Figure 11: RD006 Board Dimensions: board sides (left), board height (with 1.5 mm thick PCB) (right)

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

WÜRTH ELEKTRONIK

6 Experimental results

6.1 Experimental test setup

The reference design board prototype has been tested 'on-the-bench' and the results are given in this section. The equipment used is listed below.

6.1.1 List of equipment required (used in this case)

- 1 x Laboratory power supply (min. 40 V/0.3 A) (used EA-PSI 9040-40 T)
- 4 x 4-digit precision multimeter (used a three channel Yokogawa WT3000E precision power analyzer)
- 2 x electronic loads (min. 10 V/0.5 A) (used EA-EL 9080-45 T)
- 1 x oscilloscope (4 channel, 350 MHz or higher) (used Keysight InfiniiVision DSO-X-3034T)

NOTE: Electronic loads were used in constant-current mode. Alternatively, resistive-load mode or discrete resistors can also be used (with a value of around 15 Ω for full load on each rail).

6.1.2 System setup

The configuration of the equipment and the unit under test is shown below.

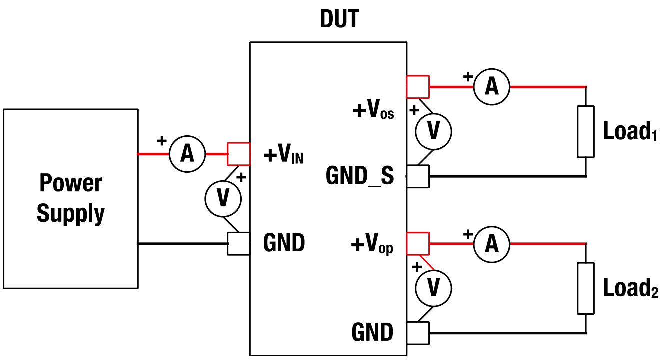

Figure 12: Example of test setup configuration

6.1.3 Designators used

In the experimental results which follow, the following designators are used:

V_{in}: Input voltage

Vop: Primary output voltage (non-isolated rail)

Vos: Secondary output voltage (isolated rail)

Iop: Primary output current (non-isolated load)

Ios: Secondary output current (isolated rail)

Vsw: Voltage on switching node

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

WÜRTH ELEKTRONIK

6.2 Voltage regulation (balanced load)

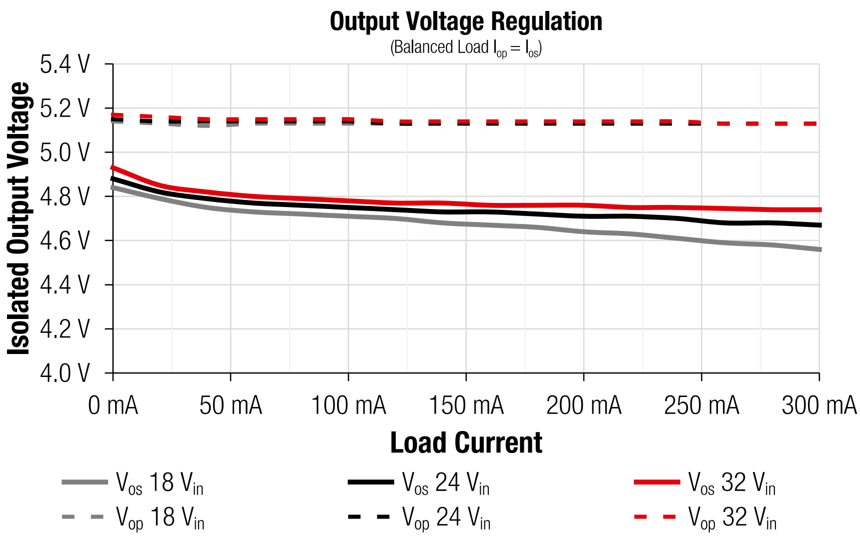

Figure 13: Voltage Regulation (at $I_{op} = I_{os}$ (balanced load))

6.3 Voltage regulation (unbalanced load: I_{op} = 300 mA (fixed))

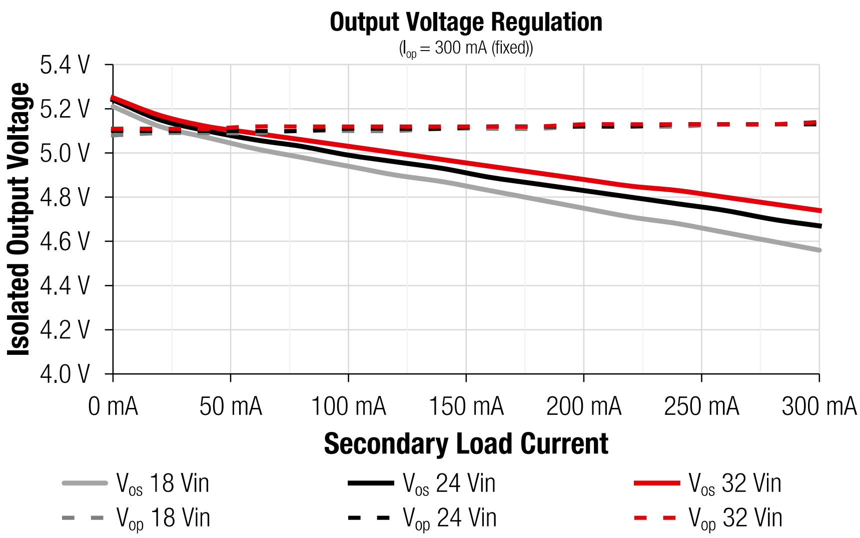

Figure 14: Voltage Regulation (at fixed I_{op} = 0.3 A (unbalanced load))

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

6.4 Voltage regulation (unbalanced load: I_{op} = no-load (fixed))

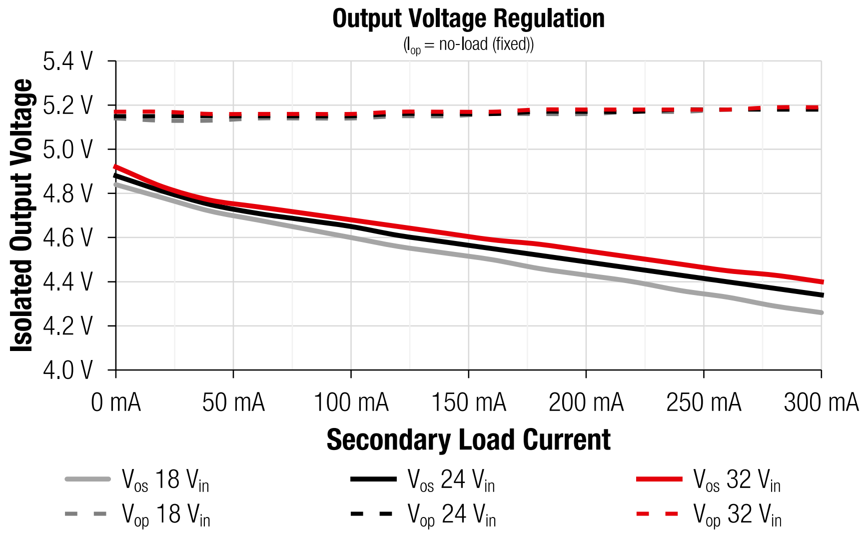

Figure 15: Voltage Regulation (at fixed I_{op} = no-load (unbalanced load))

6.5 Voltage regulation (unbalanced load: I_{os} = 300 mA (fixed))

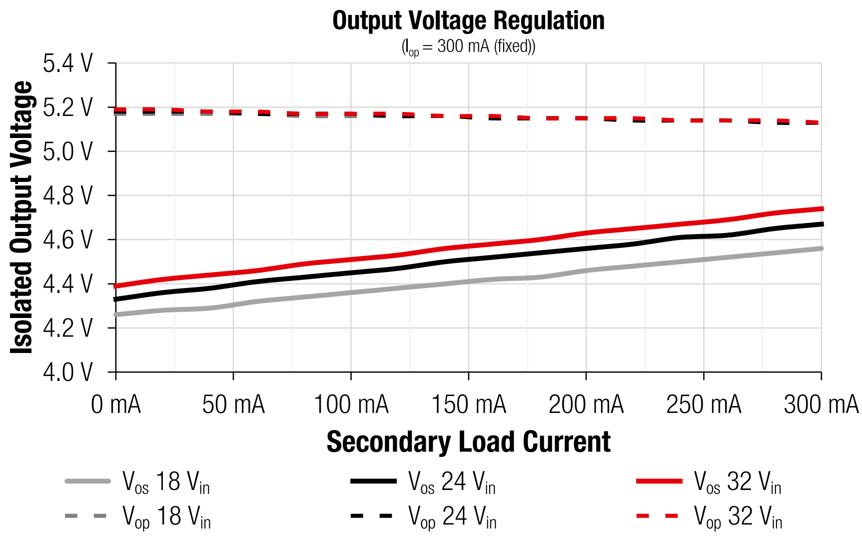

Figure 16: Voltage Regulation (at fixed I_{os} = 300 mA (unbalanced load))

6.6 Voltage regulation (unbalanced load: I_{os} = no-load (fixed))

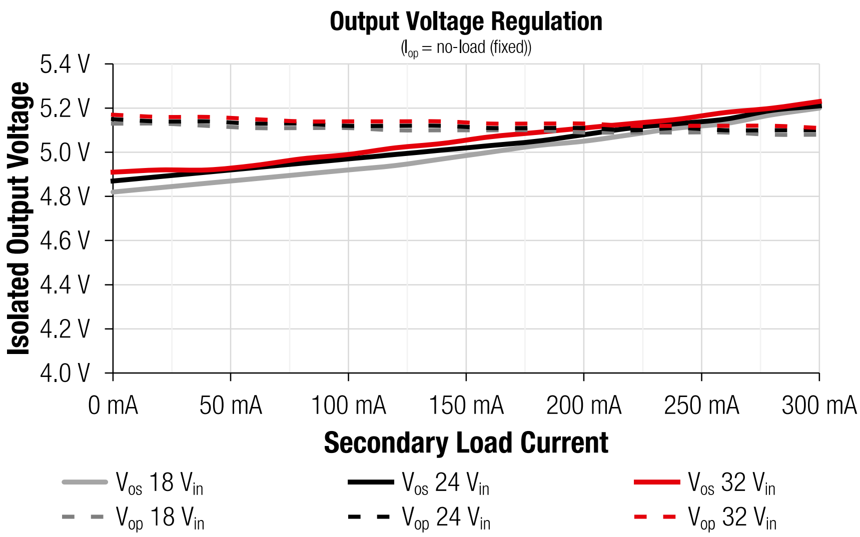

Figure 17: Voltage Regulation (at fixed I_{os} = no-load (unbalanced load))

6.7 Voltage regulation worst-case limits (unbalanced load)

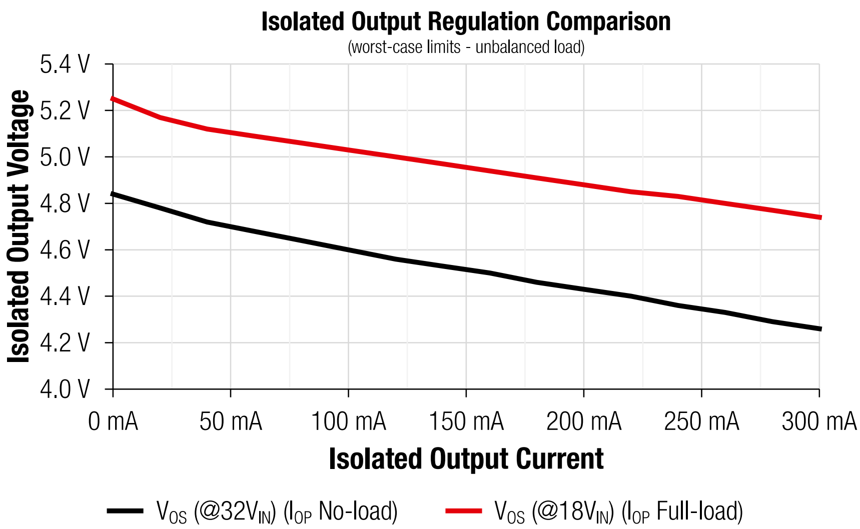

Figure 18: Voltage Regulation worst-case limits (unbalanced load)

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

6.8 Power Efficiency (balanced load)

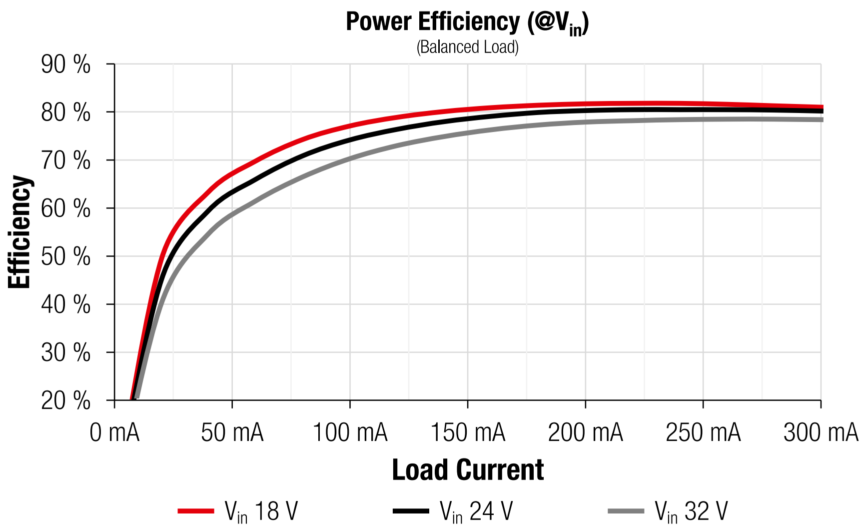

Figure 19: Power Efficiency (balanced load)

6.9 Power Efficiency (unbalanced load: Iop = 300 mA (fixed))

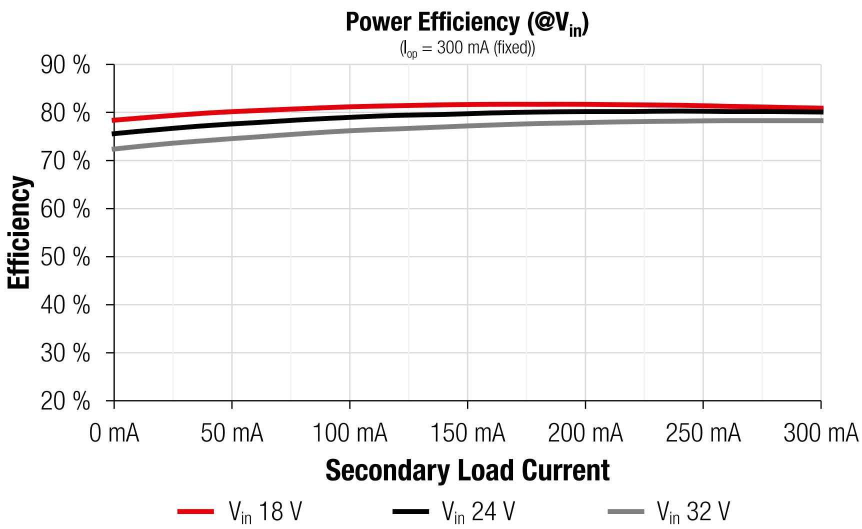

Figure 20: Power Efficiency (at fixed I_{op} = 300 mA (unbalanced load))

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

6.10 Power Efficiency (unbalanced load: I_{op} = no-load (fixed))

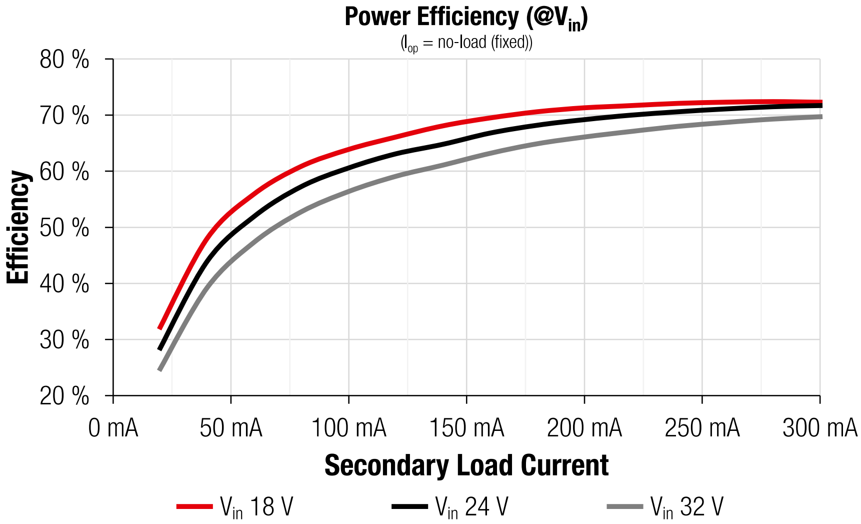

Figure 21: Power Efficiency (at fixed I_{op} = no-load (unbalanced load))

6.11 Power Efficiency (unbalanced load: Ios = 300 mA (fixed))

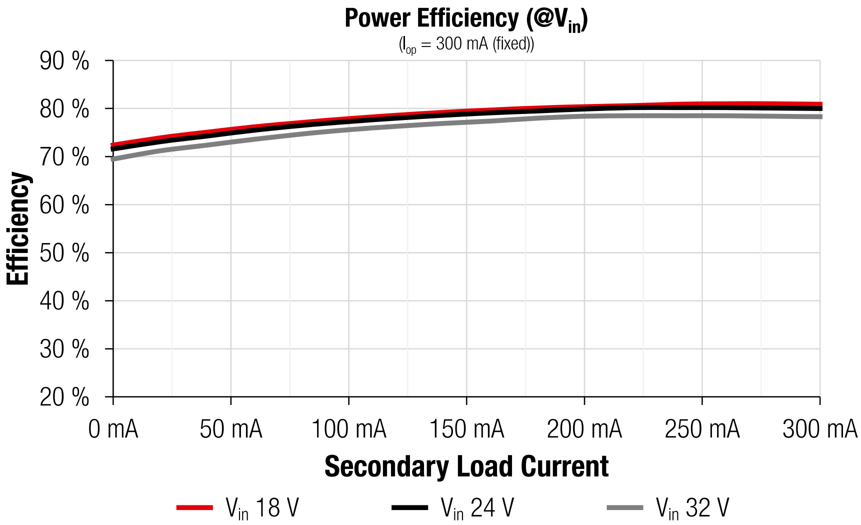

Figure 22: Power Efficiency (at fixed I_{os} = 300 mA (unbalanced load))

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

6.12 Power Efficiency (unbalanced load: I_{os} = no-load (fixed))

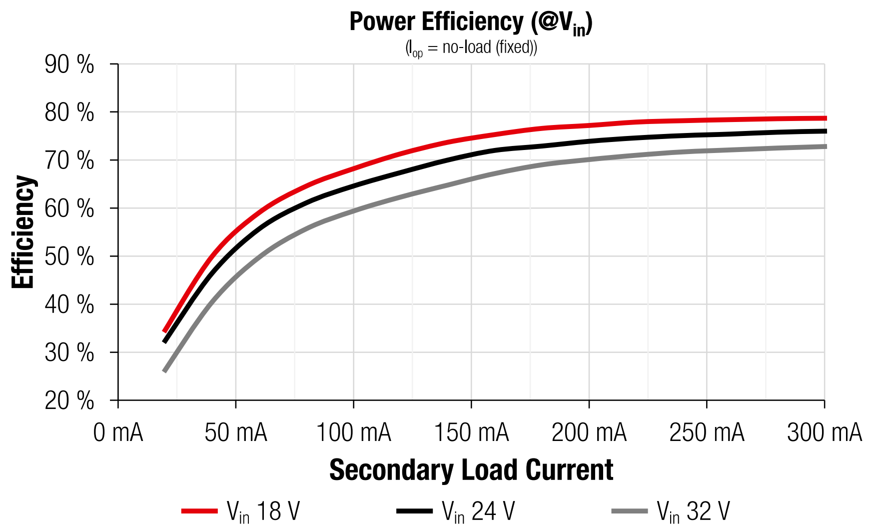

Figure 23: Power Efficiency (at fixed I_{os} = no-load (unbalanced load))

7 Main waveforms, oscilloscope captures

7.1 Start-up and Shut-down

The start-up event shows a fast ramp-up of both output supply rails with no overshoot or ringing. The small ringing observed in the input voltage step is due to the resonance between the parasitic inductance of the wire and the input capacitance of the RD006, implemented with MLCC capacitors with very low ESR, therefore with very low damping factor. During the shut-down event, the input capacitance discharges holding the voltage rails up for about 350 µs. Note that the isolated output rail starts decreasing first due to limited power as Vin reduces. Once the UVLO threshold is reached, switching stops and both output voltages fall gently to zero as the respective output capacitors deliver the remaining stored energy to the loads.

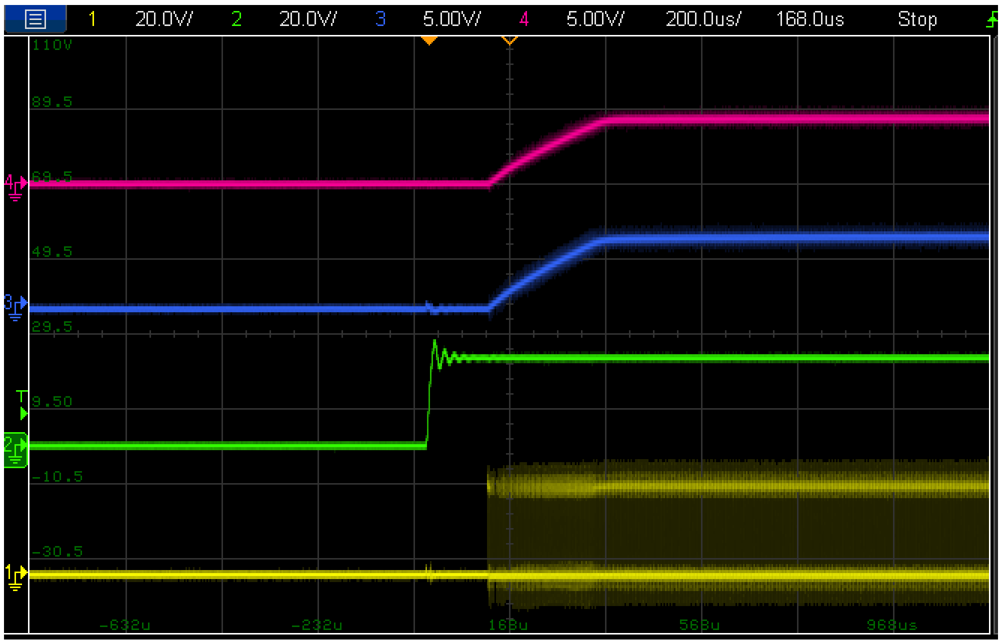

Figure 24: Start-up characteristic (V_{in} = 24 V, I_{op} = I_{os} = 300 mA (full-load, balanced))) (V_{os}, V_{op}, V_{in}, V_{SW})

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

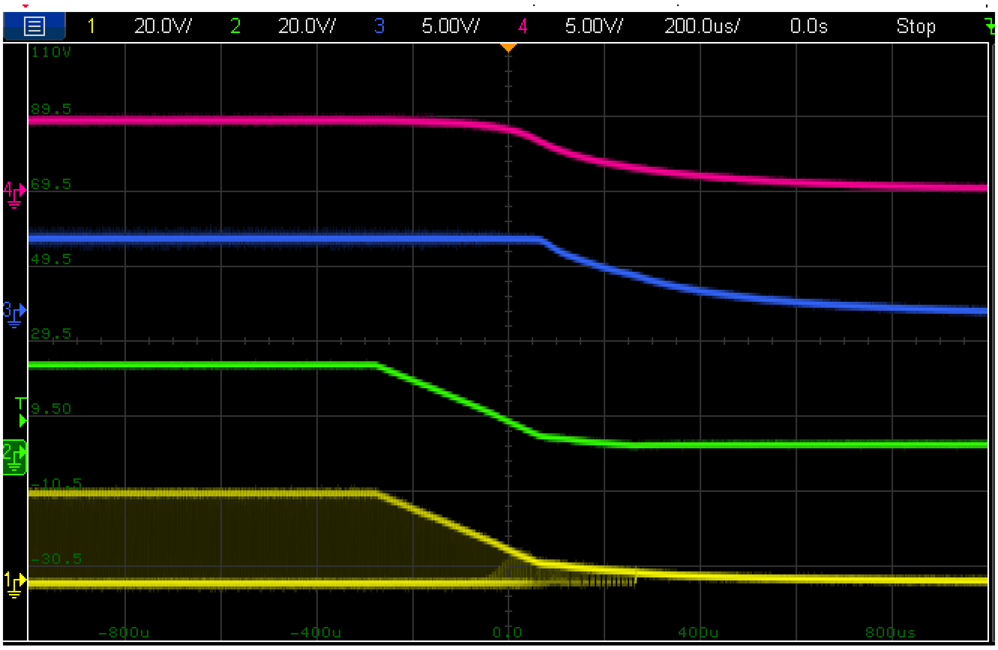

Figure 25: Shut-down characteristic (V_{in} = 24 V, I_{op} = I_{os} = 300 mA (full-load, balanced)) (V_{os}, V_{op}, V_{in}, V_{SW})

7.2 Steady-state operation

7.2.1 Full-load main waveforms (balanced)

Steady-state values of RMS and peak winding currents as well as the voltage ripple amplitude of the input and output capacitors are in line with the designed values shown in the step-by-step design of the application note ANP017.

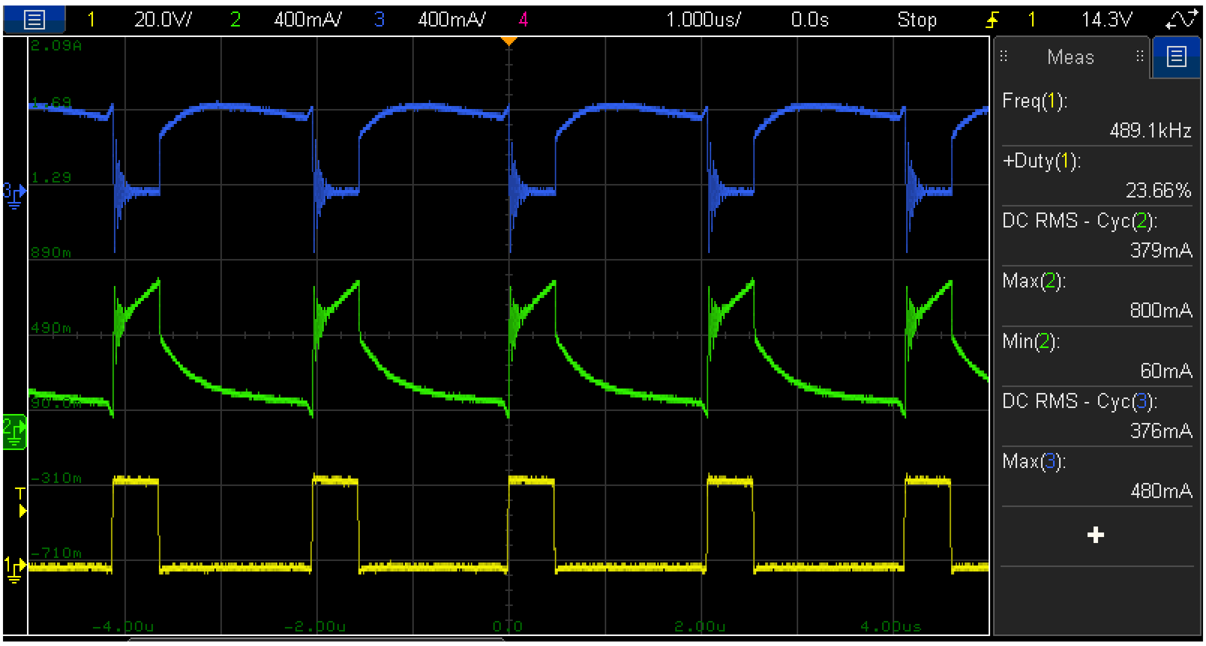

Figure 26: Winding currents and SW node voltage (@ V_{in} = 24 V, I_{op} = I_{os} = 300 mA (balanced full-load)) (I_{os}, I_{op}, V_{SW})

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

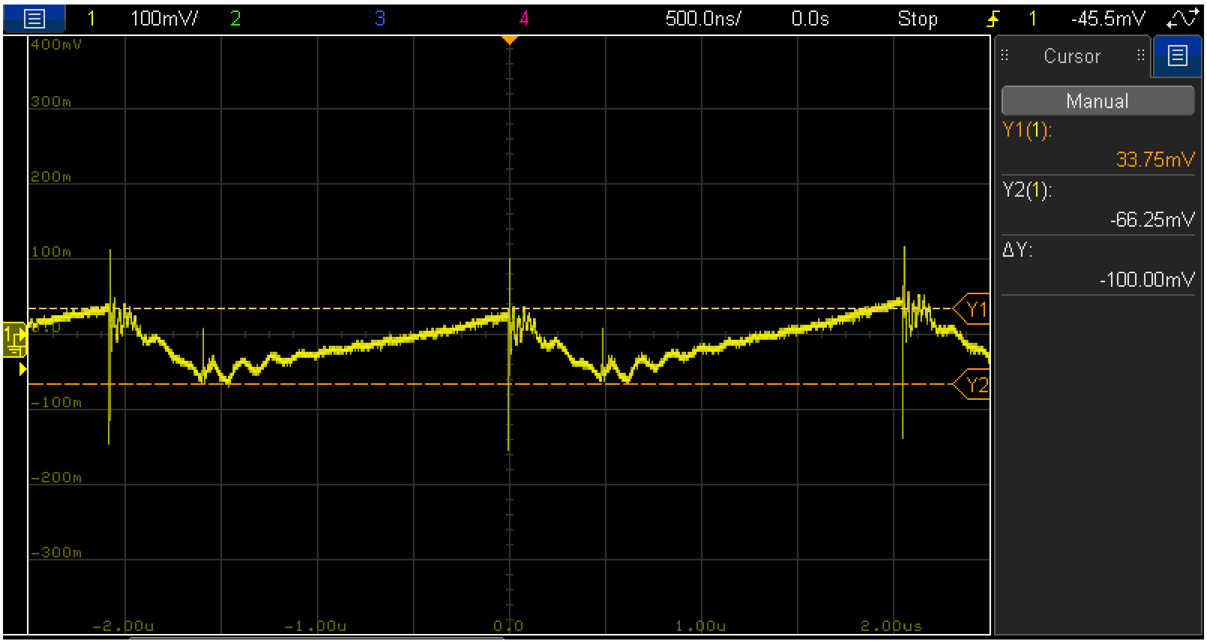

Figure 27: Input voltage ripple (@ V_{in} = 24 V, I_{op} = I_{os} = 300 mA (balanced full-load))

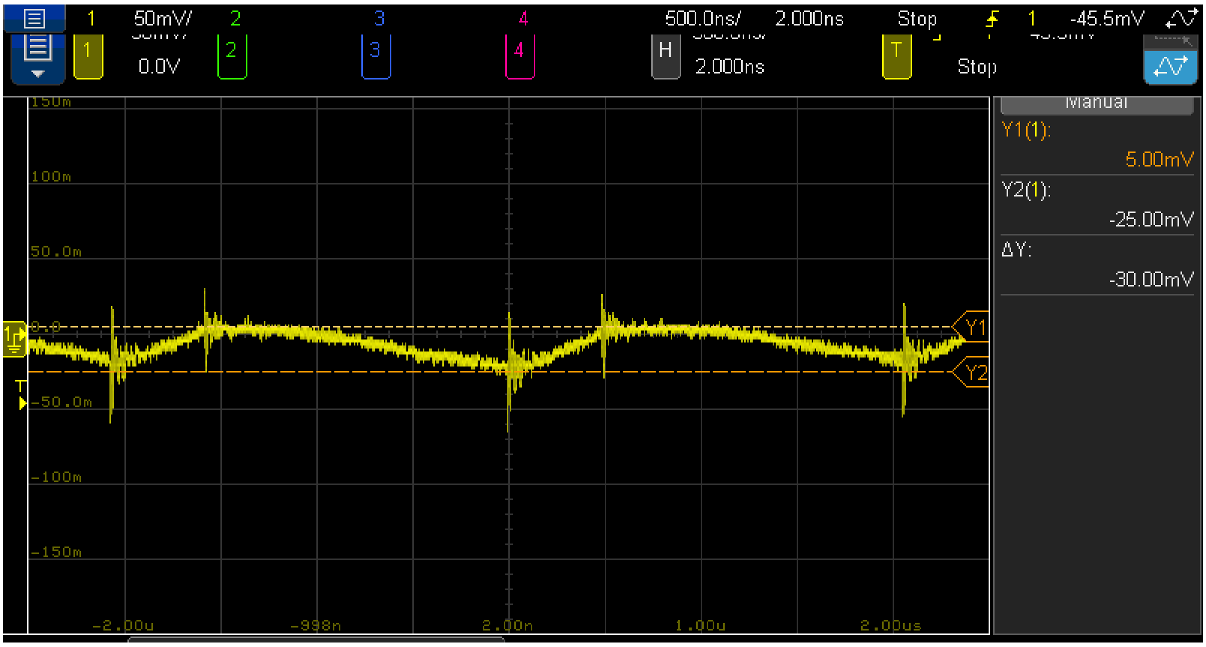

Figure 28: Primary output voltage ripple (@ V_{in} = 24 V, I_{op} = I_{os} = 300 mA (balanced full-load))

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

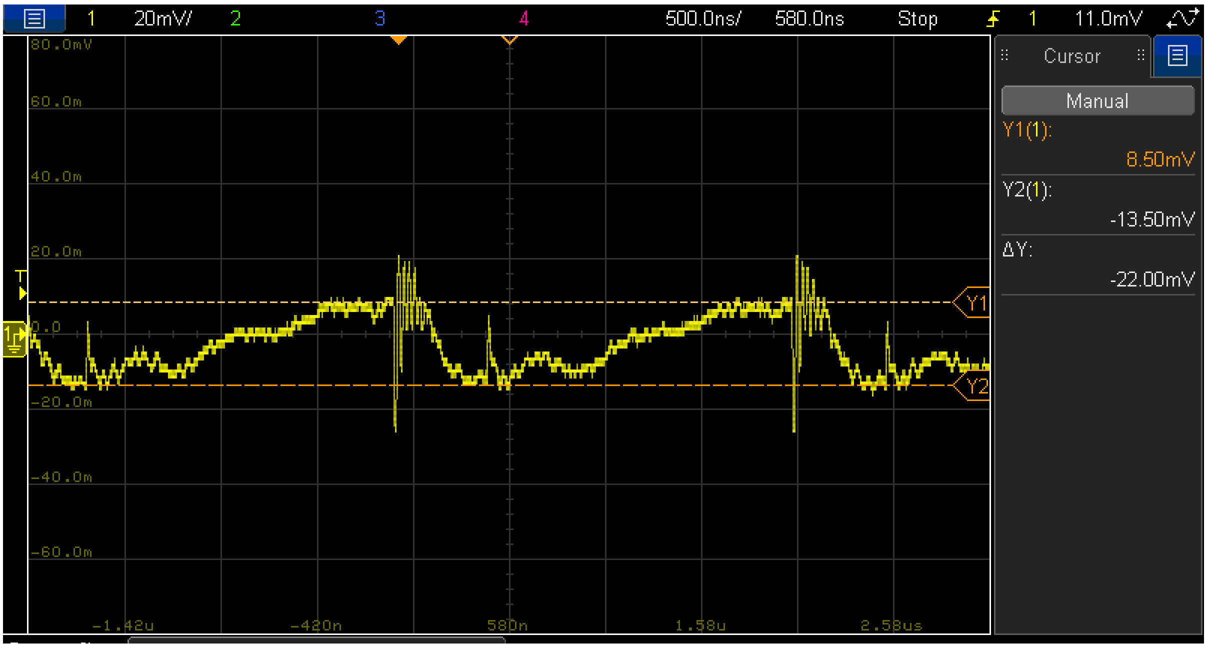

Figure 29: Secondary output voltage ripple (@ V_{in} = 24 V, I_{op} = I_{os} = 300 mA (balanced full-load))

7.3 Load transient

Load transient results have been obtained for the worst-case load current step: no-load to full-load (0.3 A) applied to one of the output rails, while holding the other rail either at no-load or at full-load. The results obtained for the four possible configurations are shown below. It is observed in all cases the small shift in the isolated output voltage level after the load current step is applied, which is expected based on the regulation curves given in previous sections 6.2 to 6.6.

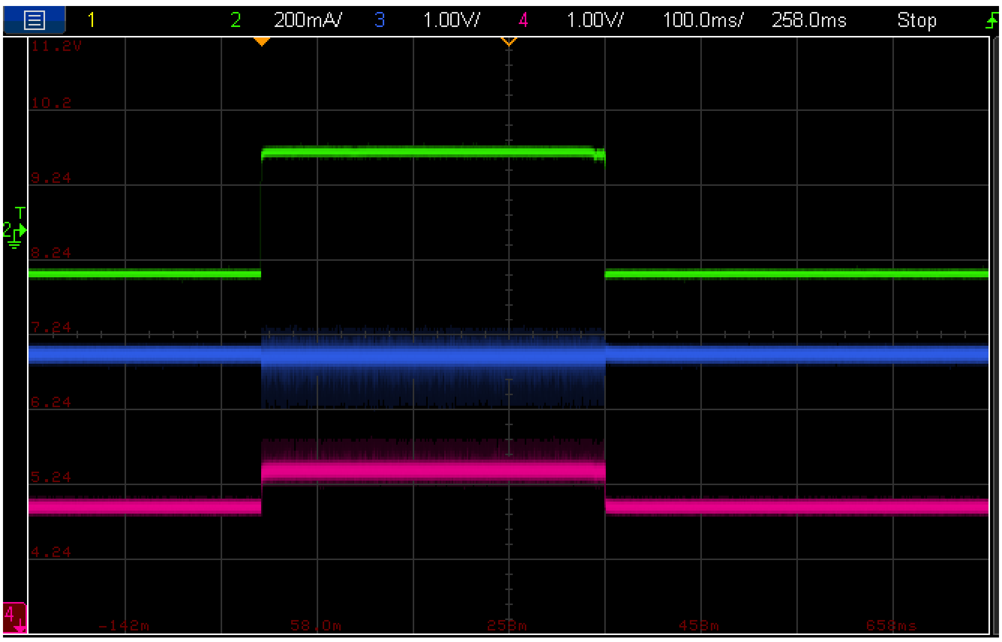

Figure 30: Load transient (I_{os} = no-load, Primary load current step 0 to 300 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

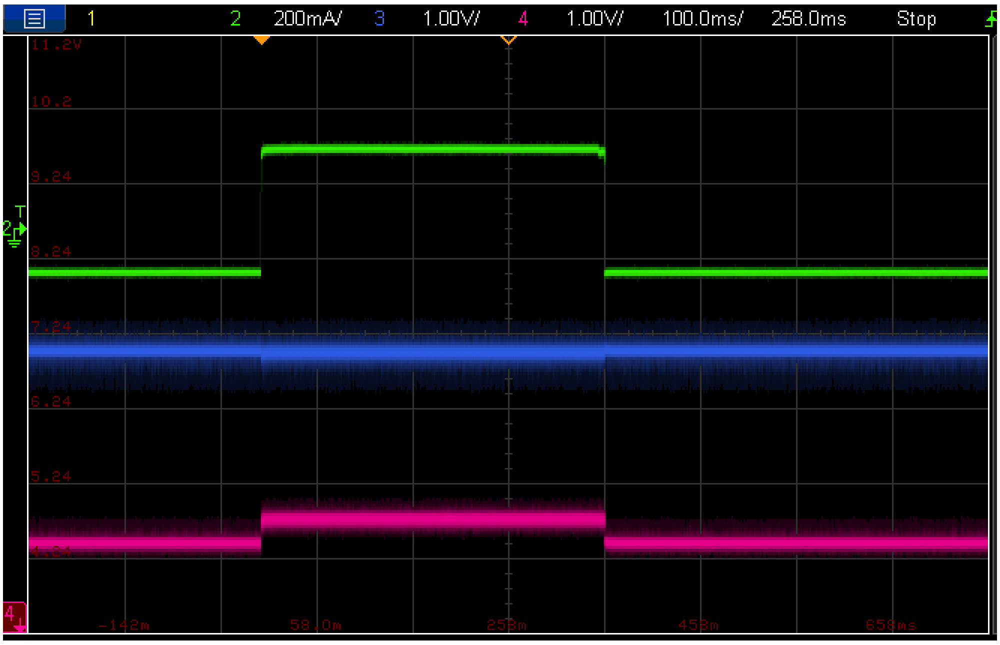

Figure 31: Load transient (I_{os} = 300 mA, Primary load current step 0 to 300 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

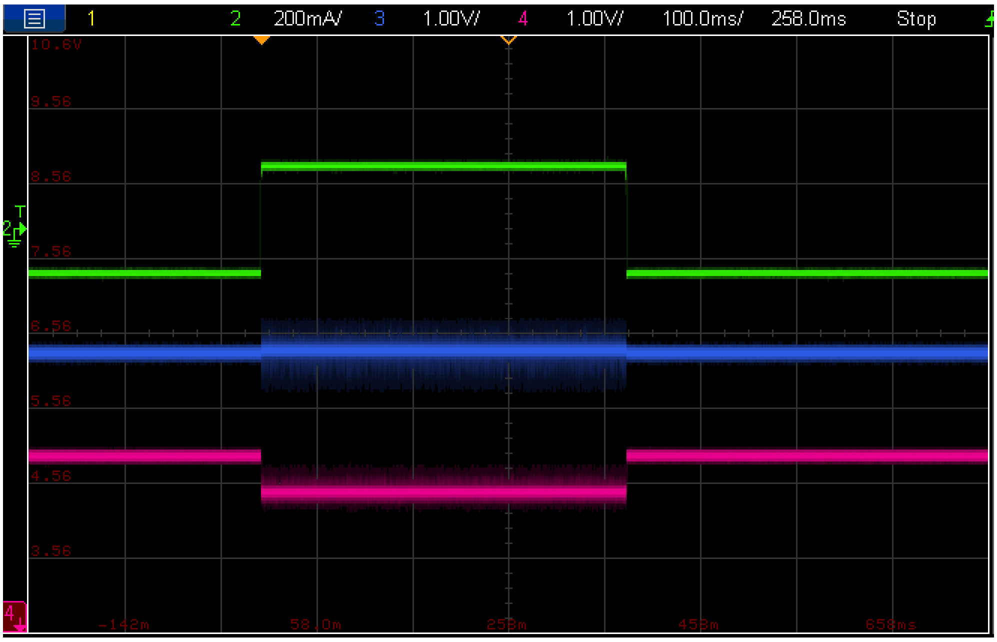

Figure 32: Load transient (I_{op} = no-load, Secondary load current step 0 to 300 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

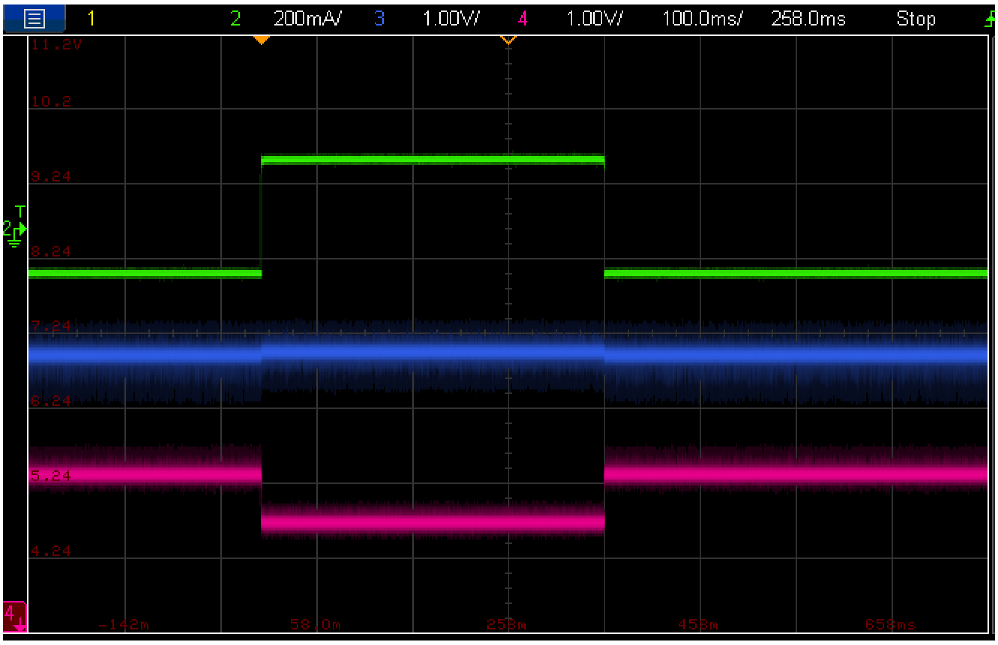

Figure 33: Load transient (I_{op} = 300 mA, Secondary load current step 0 to 300 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

A closer observation of the rising and falling current step events for one of the test conditions as example (Ios = 300 mA) reveals a slightly overdamped but fast response of the isolated output voltage without overshoot or ringing. The primary/non-isolated output voltage shows a small undershoot and overshoot of about 100 mV without ringing and a fast settling time of around 25 µs, approximately equal to that of the isolated output voltage rail. Note that for the other test conditions similar good behavior is observed.

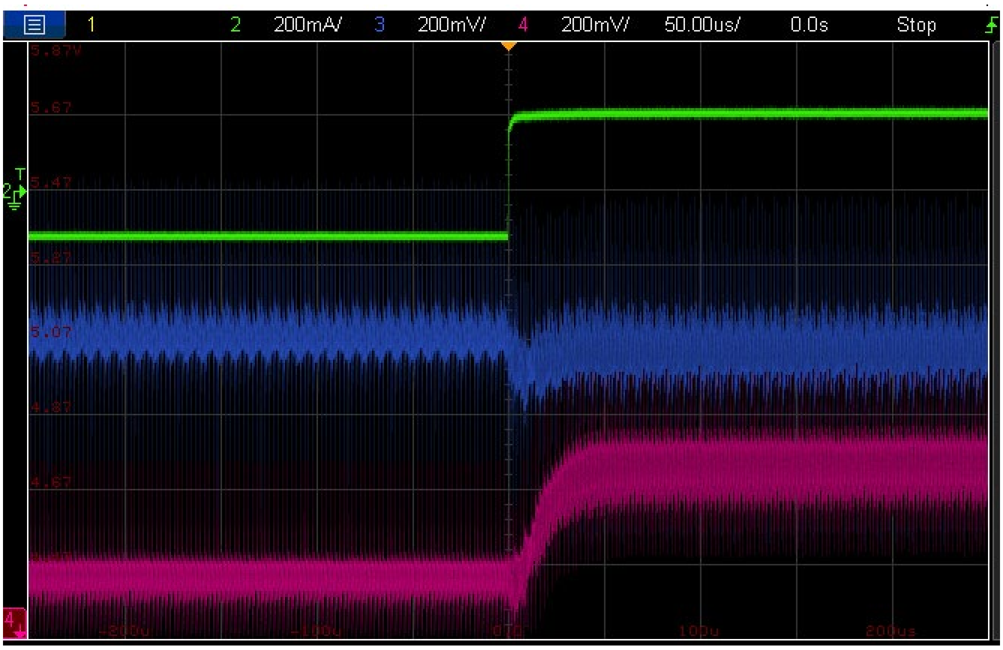

Figure 34: Load transient – Rising step (I_{os} = 300 mA, Primary load current step from 0 mA to 300 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

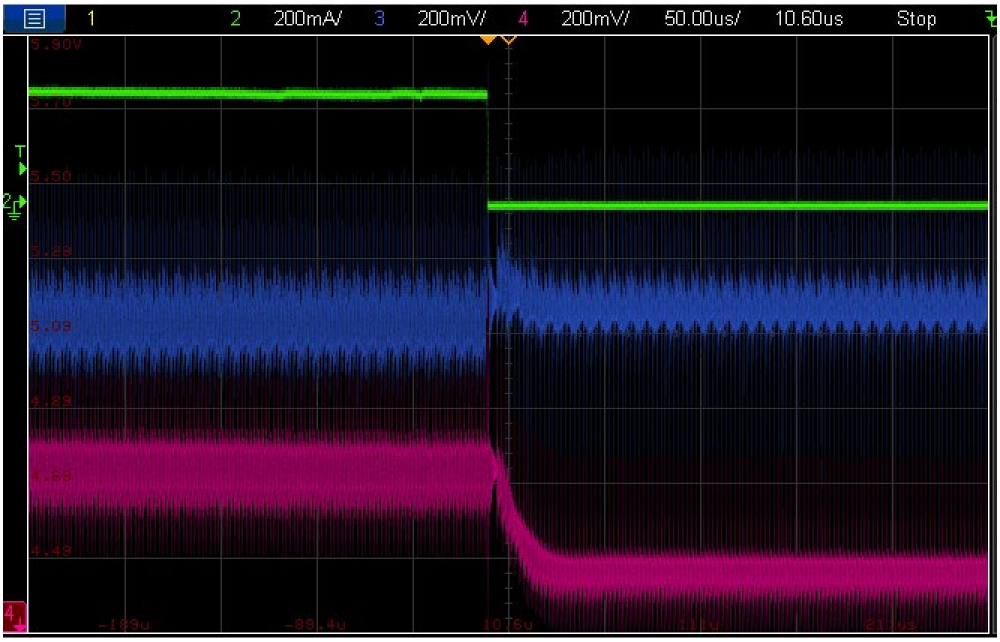

Figure 35: Load transient – Falling step (I_{os} = 300 mA, Primary load current step from 300 mA to 0 mA, 1 A/µs) (V_{os}, V_{op}, V_{in})

8 Thermal performance

Maximum component surface temperature happens at maximum input voltage and balanced full load (0.3 A on each output). Below, the results for worst-case (32 V) and for nominal input voltage (24 V) are shown.

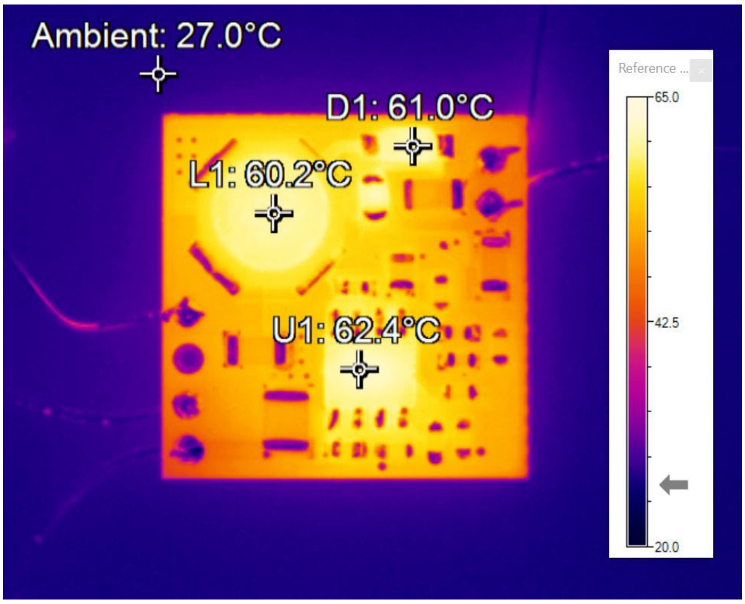

Figure 36: Board components temperature at V_{in} (max) = 32 V (worst-case) and 25 °C ambient

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

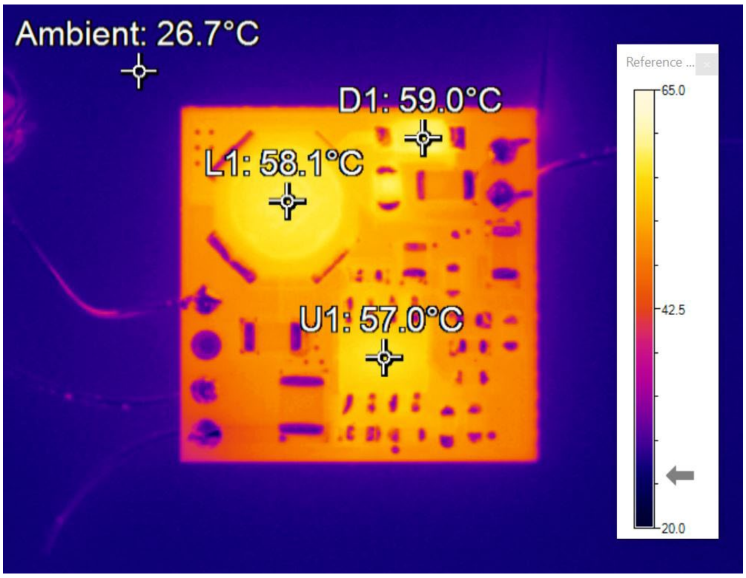

Figure 37: Board components temperature at V_{in} (nom) = 24 V and 25 °C ambient

Based on these results, and in order to keep internal/junction component temperatures within maximum ratings, it is recommended not to exceed a maximum ambient temperature of 90 °C (max) for longer lifetime and higher reliability of the application.

If this ambient temperature is exceeded, the output power must be reduced (de-rated) accordingly.

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

9 Bill-of-Materials (BoM)

Reference designator	Description	Package	Manufacturer	MPN
C1	WCAP-CSGP MLCC 4.7 µF, 50 V, X7R, 10%	1210	Würth Elektronik	885012209048
C2	WCAP-CSGP MLCC 330 nF, 50 V, X7R, 10%	0603	Würth Elektronik	885012206121
C3, C4	WCAP-CSGP MLCC 22 µF, 50 V, X7R, 10%	1206	Würth Elektronik	885012208019
C5	WCAP-CSGP MLCC 10 nF, 25 V, X7R, 10%	0603	Würth Elektronik	885012206065
C6	WCAP-CSGP MLCC 1.5 µF, 10 V, X7R, 10%	0805	Würth Elektronik	885012207023
C7	WCAP-CSGP MLCC 10 nF, 50 V, X7R, 10%	0603	Würth Elektronik	885012206089
C8	WCAP-CSGP MLCC 100 nF, 50 V, X7R, 10%	0603	Würth Elektronik	885012206095
C9	WCAP-CSGP MLCC 1 nF, 2000 V, X7R, 10%	1206	Würth Elektronik	885342208024
R1	Thick Film 127 kΩ, 0.1 W, 1 %	0603	Yageo	RC0603FR-07127KL
R2	Thick Film 15.4 kΩ, 0.1 W, 1 %	0603	Yageo	RC0603FR-0715K4L
R3	Thin Film 120 kΩ, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD07120KL
R4	Thin Film 4.7 kΩ, 0.1 W, 0.5 %	0603	Yageo	RT0603DRE074K7L
R5	Thin Film 1.5 kΩ, 0.1 W, 0.5 %	0603	Yageo	RT0603DRD071K5L
R6	Thick Film 33 kΩ, 0.1 W, 1 %	0603	Yageo	RC0603FR-1033KL
R7	Thick Film 300 Ω, 0.4 W, 5 %	0805	Vishay	RCS0805300RJNEA
D1	Schottky 60 V, 1 A	SMF	Vishay	SS1FN6-M3/H
L1	WE-TDC-HV 8038 33 µH, 1.85 A, 565 mΩ, 2 kV	SMD	Würth Elektronik	76889440330
U1	Synchronous Buck/Flybuck Controller 42 V, 0.65 A	WSON-12	Texas Instruments	LM25017MR

Table 2. RD006 Bill-of-Materials (BoM)

Reference Design

3W Isolated Bias Supply for Communication Interfaces and Measurement Systems

IMPORTANT NOTICE

USEFUL LINKS

Application Notes
www.we-online.com/app-notes

REDEXPERT Design Tool
www.we-online.com/redexpert

Toolbox
www.we-online.com/toolbox

Produkt Katalog
www.we-online.com/products

CONTACT INFORMATION

appnotes@we-online.com
Tel. +49 7942 945 - 0

Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Str. 1 · 74638 Waldenburg · Germany
www.we-online.com