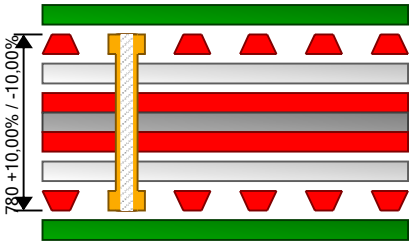
Layer	Stack up	Description	Processed Thickness	Mask Thickness	εr	Impedance ID
		Soldermask		30,00	3,50	
1		Cu-Foil	40,00			1
		1080 & 2116 TG135°	170,00		4,00	
2			33,00			
		TG 135°	250,00		4,10	
3			33,00			
		1080 & 2116 TG135°	170,00		4,00	
4		Cu-Foil	40,00			
		Soldermask		30,00	3,50	

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Target Impedance	Calculated Impedance	Tol (+/- %)	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	CI Notes-1
1		Edge Coupled Coated Microstrip 1B	1	2	0	90,00	90,32	10,00	230,00	150,00	0,00	

Drill Image	1st Layer	2nd Layer	Column Position	Drill Type	Fill Type
	1	4	2	Mechanical PTH	None

Notes

StackName: ML4_0,78_35	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 1/1	WÜRTH ELEKTRONIK
Date: 15.02.2018	Associated Documents:						
Author: Verena Laukemann							
Department:							
Site:							