

# APPLICATION NOTE

## ANP002 | The Protection of USB Applications



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### 1. INTRODUCTION

The USB-Interface might be the most distributed PC interface in the world. The usage in industry-applications is more and more common. Let's have a closer look to the special environmental conditions of industry applications. That there are real concerns regarding the robustness against EMI and ESD is written in Intel's "High Speed USB Platform Design Guidelines". Intel recommends the usage of a common mode choke for EMI suppressions and another component for protection against ESD pulses. Würth Elektronik offers all these types of products.

- The **WE-CNSW** common mode choke was developed for EMI suppression on high speed signal lines.
- For ESD suppression the TVS diode arrays **WE-TVS** with very low capacitances (< 2 pF) or the ESD Suppressors **WE-VE** (capacitances down to 0.05 pF) are your preferred choice.

But for outstanding EMI behaviour it is necessary to protect the power supply ( $V_{BUS}$ ) as well. A lot of design engineers forget this important point and wonder themselves when their product doesn't pass all the tests in EMI lab. Two typical schematics for optimized protection of one or two USB ports are shown in Figure 1 and Figure 2: With one TVS diode array **WE-TVS** you can fully protect two USB lines as well as the common power supply are well protected.

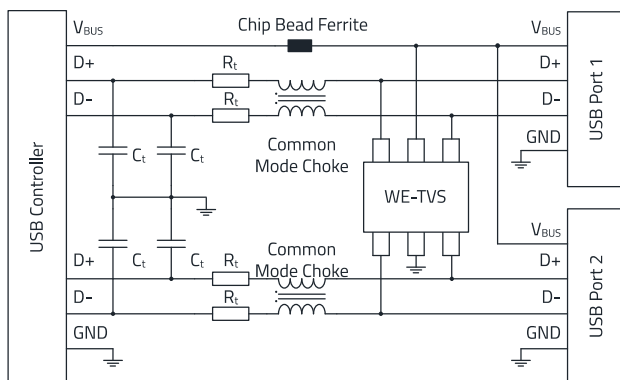


Figure 1: Two-Port-USB-Interface with ESD-Protection.

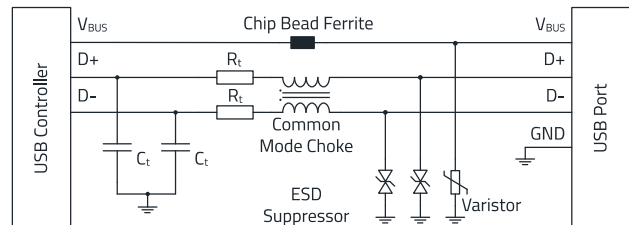


Figure 2: In contrast to the shielding of the dataline no low capacitive ESD suppressor is necessary at the power supply.

For further optimization, i.e. to filter incoming common mode noise as well as differential mode noise from USB line, a LC filter is built with the common mode choke **WE-CNSW** and the capacitors. For power supply lines very good noise suppressions can be reached with a chip bead ferrite, like the Würth Elektronik **WE-CBF** series.

Single line protection components like ESD suppressors series **WE-VE** also have to be connected from signal line to GND. For power line protection it is not necessary to use a low cap ESD suppressor, you might prefer a standard SMD varistor which can withstand higher surges and higher transient energies.

### 2. ABOUT TVS DIODES

Würth Elektronik launched the TVS diodes array series called **WE-TVS**. These TVS diodes arrays include three main functions:

- protection against ESD pulses according to EN 61000-4-2;
- protection against surge pulses according to EN 61000-4-5;
- protection against EFT pulses according to EN 61000-4-4.

**WE-TVS** series are high performance designed TVS diode arrays which include surge rated diodes. They are the best choice to protect high speed data lines like USB 2.0, DVI or LAN from over-voltages. The **WE-TVS** series exceeds the requirements outlined in EN 61000-4-2. Due to their ultra-low capacitance (< 2.0 pF) they are nearly invisible on the signal lines.

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### 3. ESD SUPPRESSOR

The ESD suppressors are special raised varistors with a low and defined intrinsic capacitance. Würth Elektronik has three different series:

- **WE-VE** standard series: Capacitances of 1 pF to 120 pF and voltages from 5 V to 24 V;
- **WE-VE** "ULC" series: Capacitance of 0.2 pF, suitable for signal lines up to 12 V;
- **WE-VE** femtoF series: Capacitance of 0.05 pF and rated voltages of 6 V, 14 V and 26 V.

For the first two series are also four-fold array packages available.

#### 3.1 Why ESD Protection?

Since the first electronic developments, all the parts are subjected to electrostatic discharge. ESD events have peak voltages up to 30kV and therewith they are very dangerous for all kind of integrated circuits. However, some state-of-the-art ICs are protected against ESD pulses but real world conditions show daily that an additional protection device is indispensable. On the one hand to have the whole board ESD free and on the other hand to develop more reliable products to satisfy the needs of your customers.

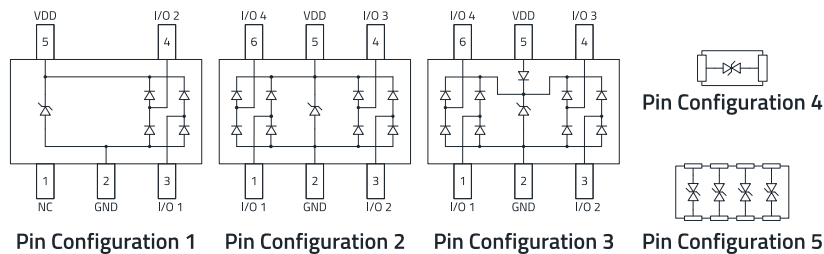


Figure 3: Several Pin-Configurations of WE-TV S series.

Order Code	Size	Pin Configuration	I/O / V <sub>DD</sub> lines	V <sub>RWM</sub>	C <sub>IN</sub>	I <sub>PP</sub>	V <sub>ESD</sub>	V <sub>ClESD</sub>	V <sub>DD</sub> can float
<b>824 011</b>	SOT23-5L	1	2 / 1	5 V	2.0 pF	12 A	20 kV	13 V	No
<b>824 002 74</b>	SC70-6L	2	4 / 1	5 V					No
<b>824 015</b>	SOT23-6L	2	4 / 1	5 V	2.0 pF	12 A	20 kV	13 V	No
<b>824 001</b>	SOT23-6L	2	4 / 1	5 V	1.0 pF	5 A	15 kV	14 V	No
<b>824 014</b>	SOT23-6L	3	4 / 1	5 V	0.5 pF	4 A	16 kV	12 V	Yes
<b>824 014 44</b>	MSOP-10L								Yes
<b>823 07 050 029</b>	0402	4	1	5 V	0.2 pF	-	8 kV	17 V	-
<b>823 06 050 029</b>	0603	4	1	5 V	0.2 pF	-	8 kV	30 V	-

Table 1: WE-TV S series comparison.

#### 3.2 Why EMI Suppression?

With the increase in electronic/electrical products and the need to have wireless connectivity in today's global markets, there is an increased requirement to ensure that your product is immune to the impacts caused by both the intentional and un-intentional RF environment. Only if you consider now which EMI phenomena impacts on the product, will you be able to design in the appropriate protection and reduce time to market. In addition, the product must not generate excessive levels of EMI and this is typically assessed by an EMC Test Laboratory, and should the product fail then costs to implement remedial work will increase aggressively.

### 4. DIFFERENT PROTECTION COMPONENTS FOR DIFFERENT APPLICATIONS

#### 4.1 How to find the Suitable Part?

- You have supply voltage to connect for rail-to-rail clamping → take TVS diode
- You don't have supply voltage or do prefer ceramic components → take TVS diode where V<sub>DD</sub> pin can float or take WE-VE ESD suppressor

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- Which maximum capacitance can you add to your data lines to pass the eye pattern test? → For USB 2.0 line capacitances up to 5 pF shouldn't cause any trouble
- What's the maximum expected ESD voltage that can occur?
- Do you want to protect one or two USB lines? However, connecting one USB data line with two I/O ports of TVS diode lets you get a better performance? → Select array type

Answer all these questions and you will find the most suitable part for you. We recommend for one USB 2.0 port [WE-TVS 824 011](#) and for two USB 2.0 ports [824 015](#).

### 5. EYE PATTERN TEST

After making a choice of protection element you have to ensure that your whole interface design meets the requirements of USB specification. Therefore you can use our protection devices with a small capacitance which is nearly invisible on the signal lines.

The eye pattern test shows that the [WE-TVS](#) do not disturb the USB 2.0 signal. You would get the same result with our other here listed TVS diodes and with the ESD suppressors as well. The following table shows the cutting edge ultra-low capacitance technology of Würth Elektronik. This new technology enables a channel to channel capacitance which is almost invisible at normal operating conditions.

Order Code	Size	I/O	V <sub>RWM</sub>	C <sub>IN</sub>	C <sub>X</sub>
<a href="#">824 015</a>	SOT23-6L	4	5	2 pF	0.1 pF
Competitor S	SOT23-6L	4	5	3 pF	1.5 pF
<a href="#">824 001</a>	SOT23-6L	4	5	1 pF	0.1 pF
Competitor P	SOT23-6L	4	5	3 pF	1.5 pF
I/O	Number of I/O lines the TVS diode can protect				
V <sub>RWM</sub>	Maximum working voltage in reverse direction				
C <sub>IN</sub>	Input capacitance I/O to GND (V <sub>IN</sub> = 2.5 V, V <sub>DD</sub> = 5 V)				
C <sub>X</sub>	Input capacitance I/O to I/O (V <sub>IN</sub> = 2.5 V, V <sub>DD</sub> = 5 V)				

Table 2: Comparison of Parts for Capacitance.

### 6. TESTING THE PROTECTION LEVEL OF ESD PROTECTION DEVICES

The easiest way to measure the protection level is to apply an ESD pulse to your electronic circuit with the ESD protection device and measure the peak voltage of this ESD pulse before and after the protection device. But this way carries out different problems. Due to high frequency and wide range of ESD pulse (few MHz to some GHz) high frequency refractions will occur during the measurement.

The absolute peak voltage and the spike voltages during the refractions are an indicator for better and worse protection, but you cannot indicate the definitive clamping voltage. And by the way, this is not a reliable and repeatable measurement! Engineers being familiar with semiconductor products do know the TLP measuring method. The TLP (transmission line pulsing) method is an accurate measurement system which allows - due to all measurements are done in a 50Ω-System - repeatable and very accurate measurements.

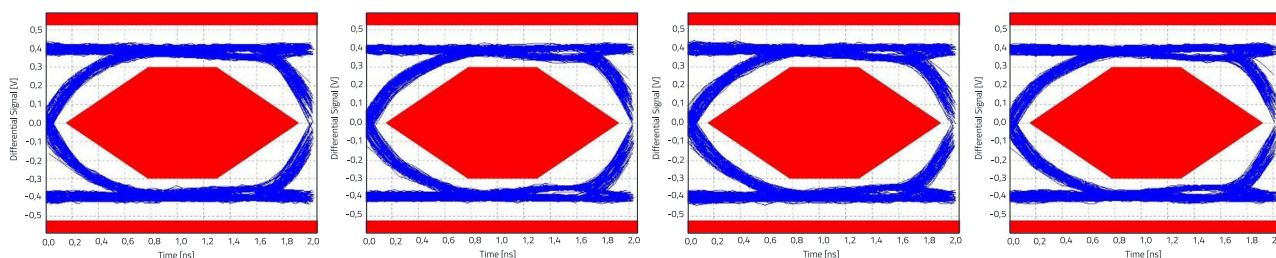


Figure 4: Eye pattern test without any protection component placed on two USB 2.0 differential signal lines.

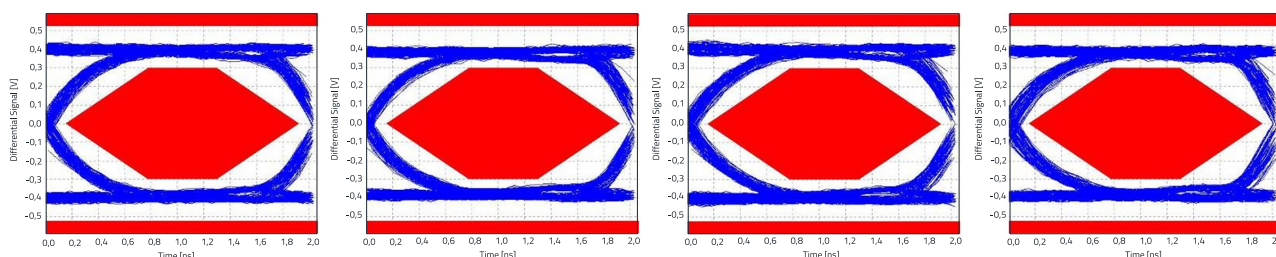


Figure 5: Eye pattern test with TVS diode WE-TVS [824 015](#).

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A defined current impulse (Figure 6 left) is charged into the protection component and the resulting voltage across it is measured (Figure 6 middle). This procedure is repeated with increasing TLP currents. As a result you get the TLP curve (Figure 6 right).

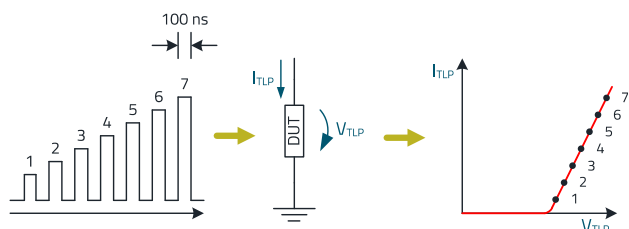


Figure 6: TLP measurement system with corresponding TLP curve.

This measurement can be done for  $V_{DD}$  and I/O pins. The lower the voltage you measure, the better is the protection device and therewith the reliability of your electronic circuit.

Thanks to the built in snap-back technology, Würth Elektronik TVS diodes have the lowest ESD clamping voltage on the market. Compared to competitors' products, the **WE-TVS** do outperform them clearly! This you can see with a short view at the TLP curves in Figure 7 and Figure 8.

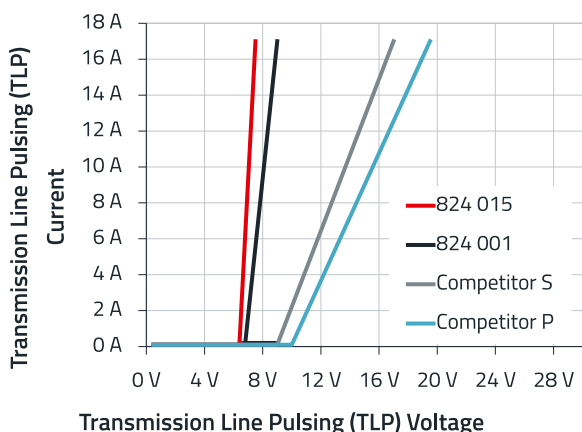


Figure 7: TLP Curve of different parts for  $V_{DD}$ .

Order Code	Size	I/O	$V_{RWM}$	$V_{Cl,I/O}$	$V_{Cl,VDD}$	$V_{ESD}$	$C_{IN}$	$I_{PP}$
<b>824 015</b>	SOT23-6L	4	5	12	7.5	12 kV	2 pF	12 A
Competitor S	SOT23-6L	4	5	22	15.5	15 kV	3 pF	12 A
<b>824 001</b>	SOT23-6L	4	5	14	9	8 kV	1 pF	5 A
Competitor P	SOT23-6L	4	5	28	19	8 kV	3 pF	6 A
I/O	Number of I/O lines the TVS diode can protect							
$V_{RWM}$	Maximum working voltage in reverse direction							
$V_{Cl,I/O}$	ESD clamping voltage at the I/O pin (IEC 61000-4-2, contact discharge, 6 kV)							
$V_{Cl,VDD}$	ESD clamping voltage at the $V_{DD}$ pin (IEC 61000-4-2, contact discharge, 6 kV)							
$V_{ESD}$	Maximum allowed ESD pulse (IEC 61000-4-2, contact discharge)							
$C_{IN}$	Input capacitance I/O to GND ( $V_{IN} = 2.5 V, V_{DD} = 5 V$ )							
$I_{PP}$	Maximum allowed pulse current (8/20 $\mu s$ )							

Table 3: Comparison of Parts for  $V_{DD}$ .

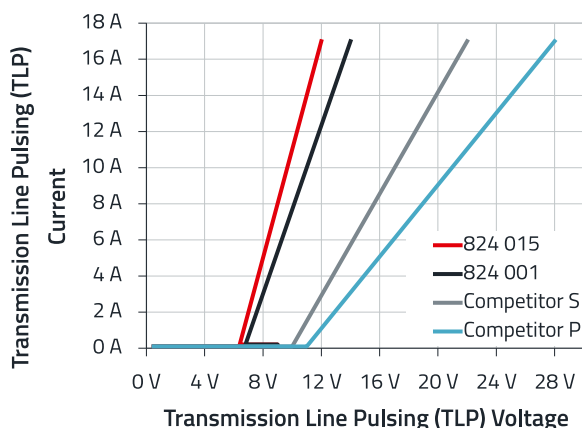


Figure 8: TLP Curve of different parts for I/O.

## 7. RECOMMENDED LAYOUT FOR SINGLE USB PORT

The two differential signal lines (D+ and D-) are routed from connector to TVS-Diode (WE-TVS **824 011**) and via a common mode choke (WE-CNSW **744 232 090**) to the USB controller as shown on Figure 9. This results in an awesome ESD protection and EMI suppression of both data lines.  $V_{BUS}$  is routed like the signal line, but instead of the common mode choke a chip bead ferrite (WE-CBF **742 792 641**) is used. After the chip bead you may add a capacitor and a second chip bead as well to get the highest possible EMI suppression effect.

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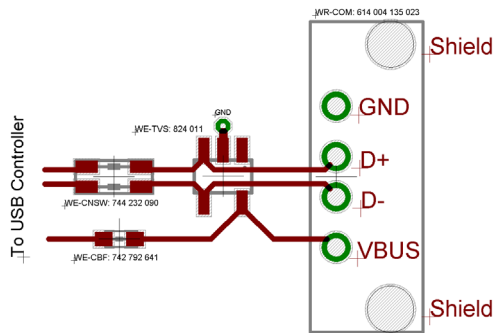


Figure 9: Protection of single USB port.

For very sensible IC's and / or high reliable applications you can get an optimized ESD suppression effect if you double contact a four-fold TVS array (WE-TVS [824 015](#)) like shown on Figure 10.

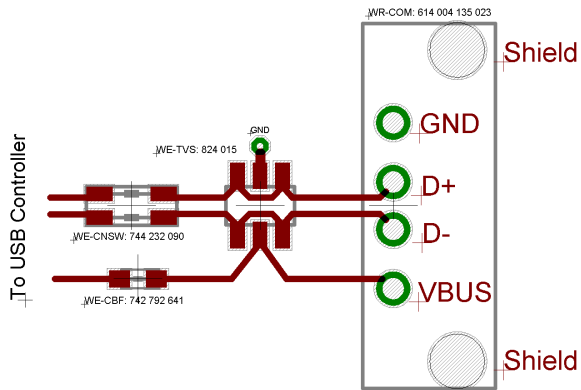


Figure 10: Double Protection of single USB port.

Designers preferring single channel components can also use the ESD Suppressors [WE-VE](#). The connection has to be carried out from D+ / D- to GND. The other parts are connected in same way as above.

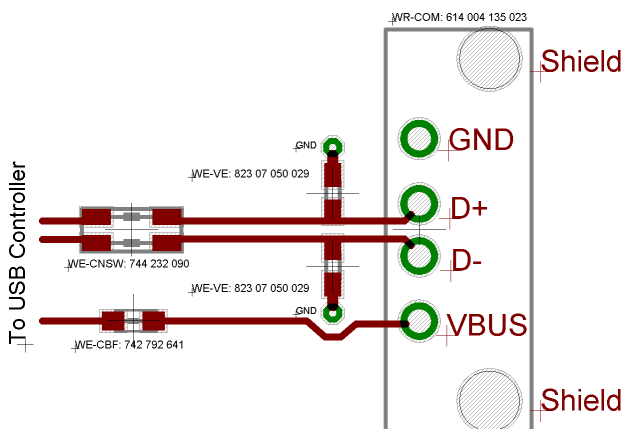


Figure 11: Protection of single USB port.

### 7.1 Recommended Layout for Double USB Port

According to single USB port protection the routing is very similar. Use here exactly the same parts as for single port protection and the protection level will also be the same.

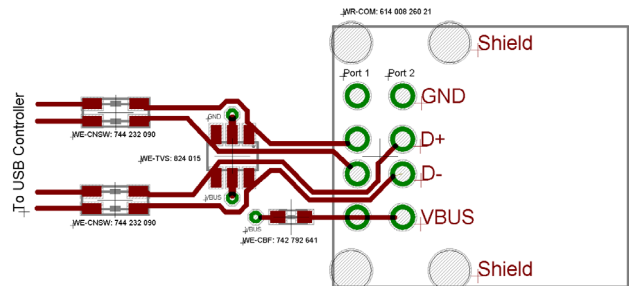


Figure 12: Protection of double USB port.

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### IMPORTANT NOTICE

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## REVISION HISTORY

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ANP002a	2010/11/25	Initial release of the application note
ANP002b	2015/03/13	Link insertion and formatting changes, disclaimer added
ANP002c	2016/08/19	Formatting changes
ANP002d	2016/04/17	Migration to a new graphic design, chapter 8 removed, minor wording changes

**Note:** The current version of the document and the release date are indicated in the footer of each page of this document.