APPLICATION NOTE

ANP015 | 1-Phase Line Filter Design

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01. INTRODUCTION

The aim of this application note is to provide the reader with a comprehensive overview of the steps necessary toward a suitably dimensioned line filter whose format is as compact as possible. A discrete single-stage line filter is compared here with a discrete two-stage line filter by means of calculation, simulation and measurement. The different core materials of the common mode chokes and their properties are then explained. This application note also addresses the calculation of: varistors, leakage currents and discharge resistors. It requires a certain knowledge of passive components, filters and EMC measurement techniques.

02. PRECOMPLIANCE MEASUREMENT SETUP

The two different interference current paths have to be distinguished: common mode (CM) and differential mode (DM). In an EMC acceptance test, both interference current paths are always measured at the same time. In the design of a line filter, it is advantageous to be able to measure both paths, CM and DM, at the outset. This requires an LISN (Line Impedance Stabilization Network) in which the two measurement outputs can be used at the same time. Two 50 Ω measuring resistors are used in the LISN. In DM measurement, they are in series (100 Ω), whereas in CM measurement they are in parallel (25 Ω). The block diagram in Figure 1 shows the DM and CM interference current paths between a flyback converter (interference source) and the LISN.

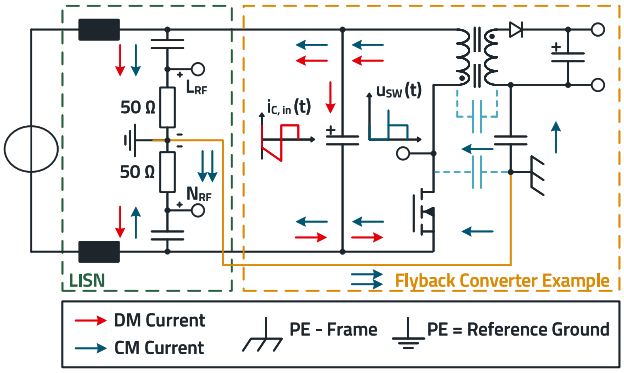

Figure 1: Simplified block diagram of a LISN, including CM and DM interference current paths, as well as an interference source (isolated flyback converter).

The two measurement outputs ($L_{,RF}$ and $N_{,RF}$) of the LISN are connected to the analog inputs 1 and 2 (50 Ω) of an oscilloscope. The mathematical function of the oscilloscope is then used to determine the interference voltage for DM and CM:

$$V_{DM} = \frac{V_{L,RF} - V_{N,RF}}{2} \quad (1)$$

$$V_{CM} = \frac{V_{L,RF} + V_{N,RF}}{2} \quad (2)$$

For precompliance measurement, a Rohde & Schwarz RTA4004 oscilloscope with 500 MHz analog bandwidth is used in conjunction with the desktop software R&S EMI Debug Tool and a CISPR16 LISN (own construction) (setup in Figure 2).

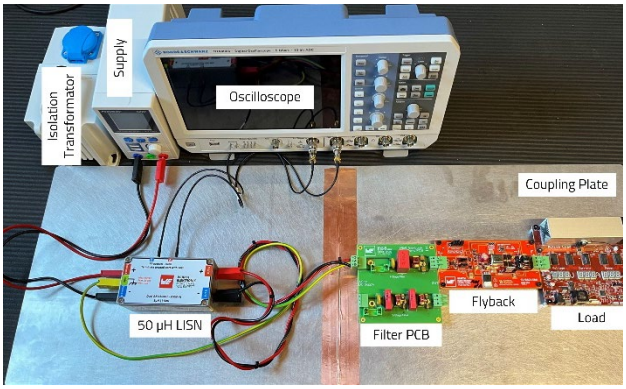

Figure 2: Precompliance measurement setup with coupling plate, LISN, DUT, isolating transformer & oscilloscope.

It should be noted that the maximum vertical resolution of the oscilloscope's measurement inputs is optimized, but that the amplitude measurement range is not overdriven. If the interference voltage measured in the time domain has a peak-to-peak level of 85 mV, for example, the vertical setting should be set to an end value of 100 mV to maximize the sensitivity of the oscilloscope (Figure 3).

Figure 3: The vertical resolution or scale of the channel is optimized, to obtain the highest sensitivity.

FFT (Fast Fourier Transformation) allows the interference spectrum in the frequency domain to be visualized from the measurement data in the time domain. The Y-axis should be set to dBµV if possible. The DUT (device under test) is then connected to the LISN without a filter and the interference spectrum is recorded. The highest interference levels are usually obtained with the maximum output load on the DUT. The common and differential mode interference specters are shown in Figure 4 and Figure 5.

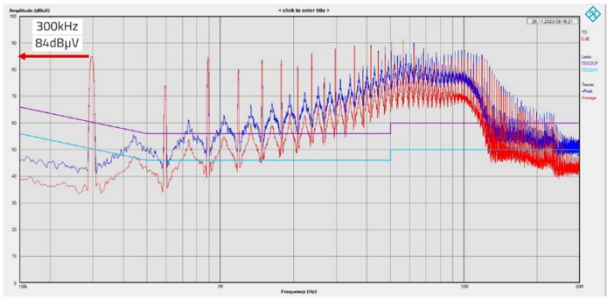

Figure 4: Common mode interference spectrum from the precompliance reference measurement of the unfiltered DUT. At the switching frequency of 300 kHz, the limit value of 50 dBµV is exceeded by both the average and quasi-peak levels of 84 dBµV in each case. So at least 34 dB of common mode insertion loss is required at the switching frequency.

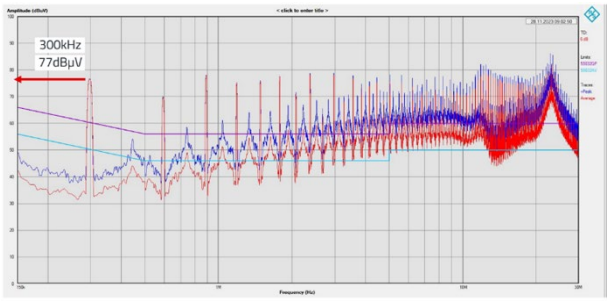

Figure 5: Differential mode interference spectrum from the precompliance reference measurement of the unfiltered DUT. At the switching frequency of 300 kHz, the limit value of 50 dBµV is exceeded by the average and quasi-peak levels of 84 dBµV in each case. So at least 27 dB of differential mode insertion loss is required at the switching frequency.

If no LISN is available whose measurement outputs can be used in parallel, the combined display of the CM and DM interference spectrum in Figure 6 is used as the basis. If no precompliance measurement is possible at the outset, the filter should be designed for at least 40 dB insertion loss (CM and DM) for the switching frequency of the power supply.

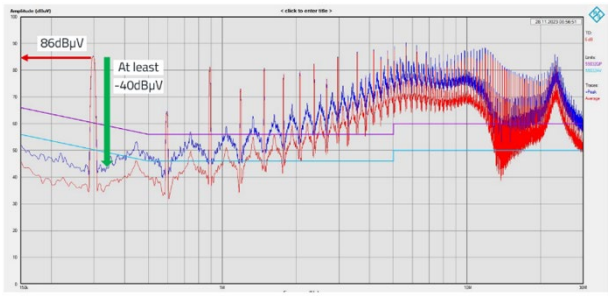

Figure 6: Combined differential mode (DM) and common mode (CM) reference measurement (precompliance) of the DUT without filter. The average and quasi-peak levels are 86 dBµV (limit bei 300 kHz: 50 dBµV). Over 36 dB of insertion loss is required at the switching frequency.

03. CALCULATION FOR THE SINGLE-STAGE LINE FILTER

If over or under dimensioning of the line filter is to be avoided at the outset, in most cases a reference measurement of the DUT **without** a filter is imperative. For this demonstration, an isolated flyback converter with 300 kHz switching frequency and 25 W maximum output power is used. This isolated power supply unit already causes very high CM and DM interference at the switching frequency. The aim of the filter design is to comply with the Class B limit values (e.g., CISPR 11, CISPR 32).

As shown in the precompliance measurements above, at least 40 dB of filter insertion loss is required at the switching frequency, which includes a safety buffer (approx. 10 dB). If the switching frequency is below the relevant EMC spectrum, you can be guided by the first relevant harmonic found in the spectrum. For example, if a power supply unit has a switching frequency of 70 kHz, then the third harmonic at 210 kHz is relevant if the EMC spectrum is measured above 150 kHz.

Single-stage LC filters (= 2nd order filters) , as shown in Figure 7 and Figure 8, enable an insertion loss of 40 dB / decade.

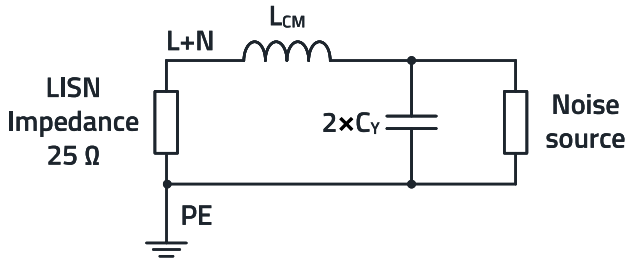

Figure 7: Simplified block diagram with the effective CM components of the single-stage filter.

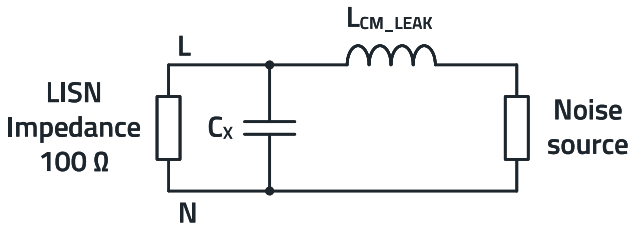

Figure 8: Simplified block diagram with the effective DM components of the single-stage filter.

The necessary filter cut-off frequency (f_{CO}) to obtain the desired attenuation (A_{fsw}) at the switching frequency (f_{SW}) can be calculated as follows:

$$A_{fsw} = \log\left(\frac{f_{sw}}{f_{CO}}\right) \cdot 40\ \text{dB} \quad (3)$$

$$f_{CO} = \frac{f_{sw}}{10^{\frac{A_{fsw\,(dB)}}{40\ \text{dB}}}} \quad (4)$$

Based on the reference measurements, it is known that an insertion loss of approximately 40 dB at f_{SW} is required for both CM and DM in order to comply with the limit values.

$$f_{CO} = \frac{300\ \text{kHz}}{10^{\frac{40\ \text{dB}}{40\ \text{dB}}}} = 30\ \text{kHz} \quad (5)$$

Next, the capacitance values for the Y-capacitors are defined. On account of the maximum permissible leakage currents (see Section 08), their capacitance values are greatly limited for many AC applications.

In this example for the single-stage filter, two 4.7 nF Y2 WCAP - CSSA ceramic capacitors are used. They are connected in parallel in the CM analysis.

$$C_{YG} = 2 \cdot C_Y = 2 \cdot 4.7\ \text{nF} = 9.4\ \text{nF} \quad (6)$$

The required common mode inductance L_{CM} of the common mode choke is then calculated:

$$L_{CM} = \frac{1}{(2\pi \cdot f_{CO})^2 \cdot C_{YG}} \quad (7)$$

$$L_{CM} = \frac{1}{(2\pi \cdot 30\ \text{kHz})^2 \cdot 9.4\ \text{nF}} = 3\ \text{mH}$$

3 mH is not a typical standard value, hence a **3.3 mH** WE - CMB "S" package is selected. As common mode chokes have a relatively high inductance tolerance, a safety buffer should always be considered. As a result of the 0.3 mH higher L_{CM} inductance, the calculated CM insertion loss is 41 dB.

Next, the leakage inductance L_{CM_LEAK} of the common mode choke is determined. If this is not specified in the data sheet, it can easily be found from the differential mode impedance curve. As can be seen in Figure 9 REDEXPERT offers an easy way to determine the impedance at a desired frequency by placing a cursor.

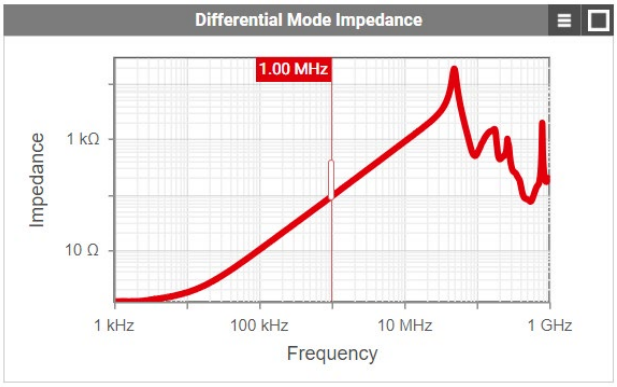

Figure 9: DM Impedance curve for the WE - CBM choke 744822233, in REDEXPERT.

The value should always be read off in the linear, ascending (= inductive) region of the curve for this purpose.

With the cursor at 1 MHz, an impedance of 92 Ω is read off.

$$L_{DM} = \frac{X_L}{2\pi \cdot f_{DM}} = \frac{92\ \Omega}{2\pi \cdot 1\ \text{MHz}} = 14.6\ \mu\text{H} \quad (8)$$

The required capacitance of the X-capacitor can then be calculated:

$$C_X = \frac{1}{(2\pi \cdot f_{CO})^2 \cdot L_{DM}} \quad (9)$$

$$C_X = \frac{1}{(2\pi \cdot 30\ \text{kHz})^2 \cdot 14.6\ \mu\text{H}} = 1.92\ \mu\text{F}$$

As no nominal 1.92 µF capacitor exists, a 2.2 µF / 310 V X2 WCAP - FTXX is used. As a result of the 0.28 µF higher capacitance, the calculated differential mode insertion loss is 41 dB. As X-capacitors can degrade markedly in practice over their lifetime due to poor mains quality (surge pulses), it is advisable to always include a safety buffer here too.

04. CALCULATION FOR THE TWO-STAGE LINE FILTER

A two-stage filter in Figure 10 and Figure 11 has four essential advantages over a single-stage filter:

- The individual components have a smaller package
- The parasitic properties (especially self-resonance) are better
- Increased design flexibility
- 80 dB / decade insertion loss as compared to 40 dB / decade

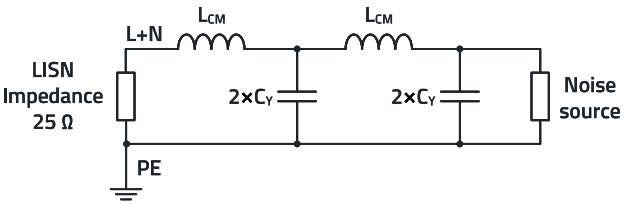

Figure 10: Simplified block diagram with the effective CM components of the two-stage filter.

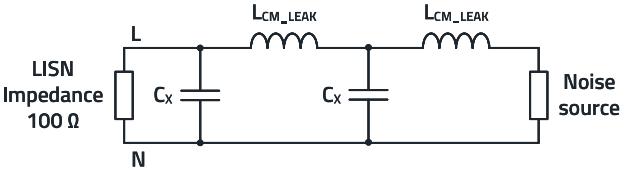

Figure 11: Simplified block diagram with the effective DM components of the two-stage filter.

To calculate the effective filter cut-off frequency (f_{CO}) required to achieve the desired attenuation (A_{fsw}) at the switching frequency (f_{SW}):

$$A_{fsw} = \log\left(\frac{f_{sw}}{f_{CO}}\right) \cdot 80\ dB \qquad (10)$$

$$f_{CO} = \frac{f_{sw}}{10^{\frac{A_{fsw\ (dB)}}{80\ dB}}} \qquad (11)$$

It is known from the reference measurements that approximately 40 dB insertion loss is required for the two interference current paths at the switching frequency f_{SW} in order to comply with the limit values..

$$f_{CO} = \frac{300\ kHz}{10^{\frac{40\ dB}{80\ dB}}} = 95\ kHz \qquad (12)$$

This is the 'effective cut-off frequency' (f_{CO}). To simplify the subsequent calculations, this effective cut-off frequency is used for further calculations. As can be seen in the following simulation, there are two different cut-off frequencies (f_{CO1} and f_{CO2}). These can be determined as follows:

$$f_{CO1} \approx 0.6 \cdot f_{co} = 0.6 \cdot 95\ kHz = 57\ kHz \qquad (13)$$

$$f_{CO2} \approx 1.6 \cdot f_{co} = 1.6 \cdot 95\ kHz = 152\ kHz \qquad (14)$$

In order for the simplified attenuation analysis (80 dB / decade) to be applicable at the effective cut-off frequency, the lowest relevant frequency (= switching frequency) should be significantly greater than f_{CO2}, so its resonance overshoot plays a less significant role.

In general, the cut-off frequencies of a two-stage filter should be at least one octave apart (frequency ratio 2 : 1) in order to avoid the resonance peaks overlapping.

As can be seen from the two equations for f_{CO1} and f_{CO2}, this condition is automatically fulfilled for a filter with the same components on both stages.

In this example, two 2.2 nF Y2 WCAP - CSSA ceramic capacitors are used.

$$C_{YG} = 2 \cdot C_Y = 2 \cdot 2.2\ nF = 4.4\ nF \qquad (15)$$

You then calculate the required common mode inductance L_{CM} of the common mode choke:

$$L_{CM} = \frac{1}{(2\pi \cdot f_{CO})^2 \cdot C_{YG}} \qquad (16)$$

$$L_{CM} = \frac{1}{(2\pi \cdot 95\ kHz)^2 \cdot 4.4\ nF} = 0.64\ mH$$

Since an inductance value of 0.64 mH is not a typical standard value and the tolerance of the choke inductance needs to be taken into account, a CM choke with an inductance value of **1 mH** from the WE - CMB series with "XS" package is selected. Due to the 0.36 mH higher inductance, the common mode insertion loss is calculated as **48 dB.**

The diagram from REDEXPERT in Figure 12 can be used to read the differential mode impedance.

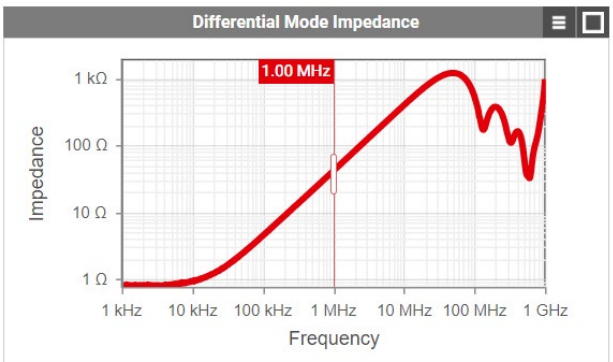

Figure 12: DM impedance curve in REDEXPERT of the WE - CMB 744821201.

With the cursor at 1 MHz, an impedance of 41 Ω is read off.

$$L_{DM} = \frac{X_L}{2\pi \cdot f_{DM}} = \frac{41\ \Omega}{2\pi \cdot 1\ \text{MHz}} = 6.5\ \mu\text{H} \qquad (17)$$

The required capacitance of the X-capacitor can then be calculated:

$$C_X = \frac{1}{(2\pi \cdot f_{CO})^2 \cdot L_{DM}} \qquad (18)$$

$$C_X = \frac{1}{(2\pi \cdot 95\ \text{kHz})^2 \cdot 6.5\ \mu\text{H}} = 0.43\ \mu\text{F}$$

As no nominal 0.43 µF capacitor exists, a 560 nF / 310 V X2 WCAP - FTXX capacitor is used. Due to the 130 nF higher capacitance, a differential insertion loss of **45 dB** is calculated.

05. CIRCUIT DIAGRAM, PCB, SIMULATION SINGLE-STAGE & TWO-STAGE LINE FILTER WITH LTSPICE

In order to implement the calculations in practice, the circuit board in Figure 14 with both filter variants is constructed for comparative measurements. Figure 13 shows the associated schematic.

The varistor calculated in Section 07 is also assembled on the circuit board. This has a parasitic capacitance of approx. 420 pF, which is taken into account in the LTspice simulation created in DM.

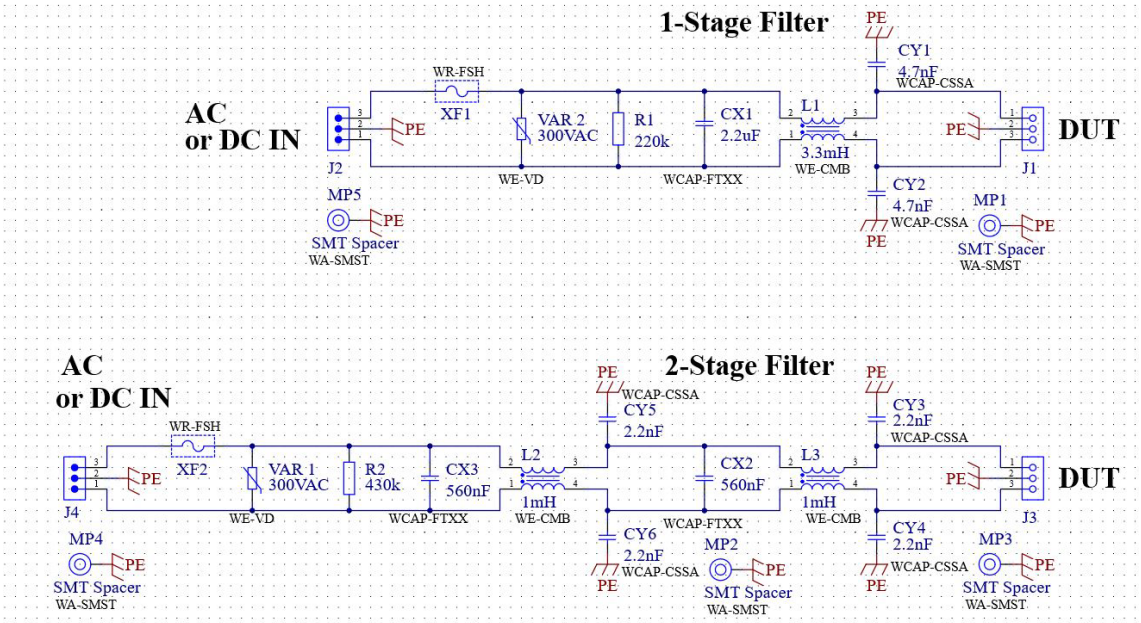

Figure 13: Altium circuit diagram with all components used.

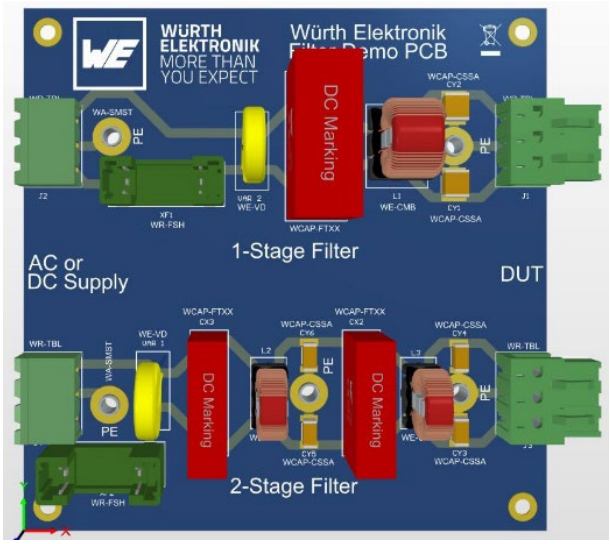

Figure 14: Altium 3D PCB with all components used.

The schematics for the LTspice simulation are shown in Figure 15 and Figure 16. In addition, the Y-capacitors in DM are in series between L & N. As these capacitors only play a role in the higher frequency spectrum, their influence is neglected in the calculation, but are taken into account in the LTspice simulation.

The simulation (Figure 17) shows that with both filters an insertion loss in CM of approx. 40 - 43 dB is achieved at the frequency of 300 kHz as in the calculation. However, from as low as 350 kHz, the two-stage filter achieves broadband filtering up to 30 dB in greater than the single-stage filter.

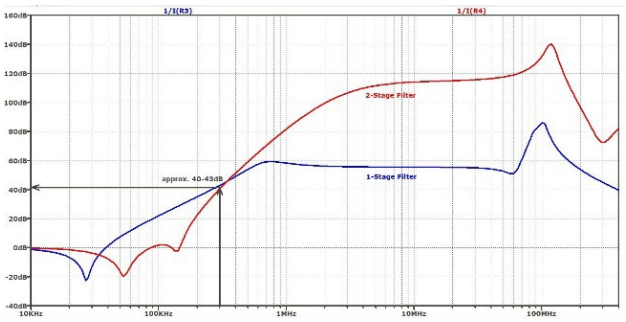

*Figure 17: LTspice simulation of **CM** insertion loss, 10 kHz to 400 MHz; blue = single-stage filter; red = Two- stage filter.*

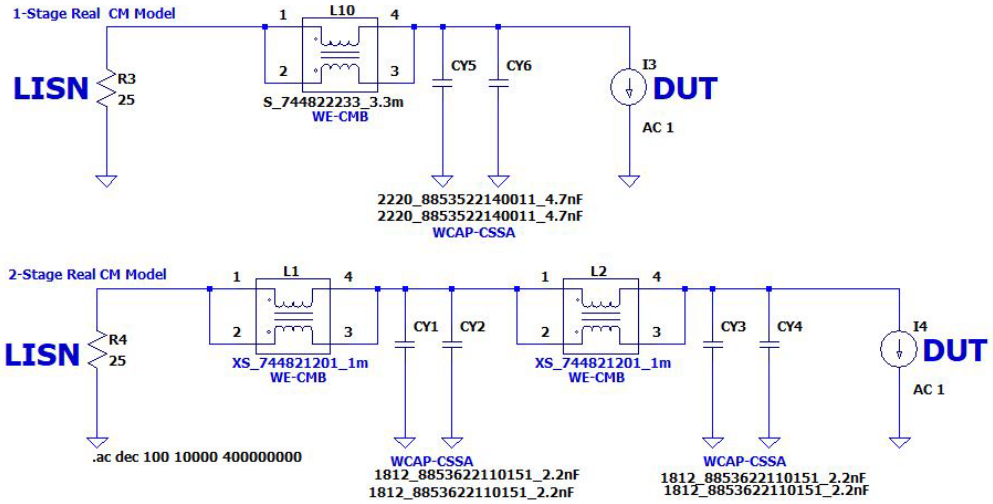

*Figure 15: LTspice circuit diagram for simulation of **CM** insertion loss with Würth Elektronik LTspice models.*

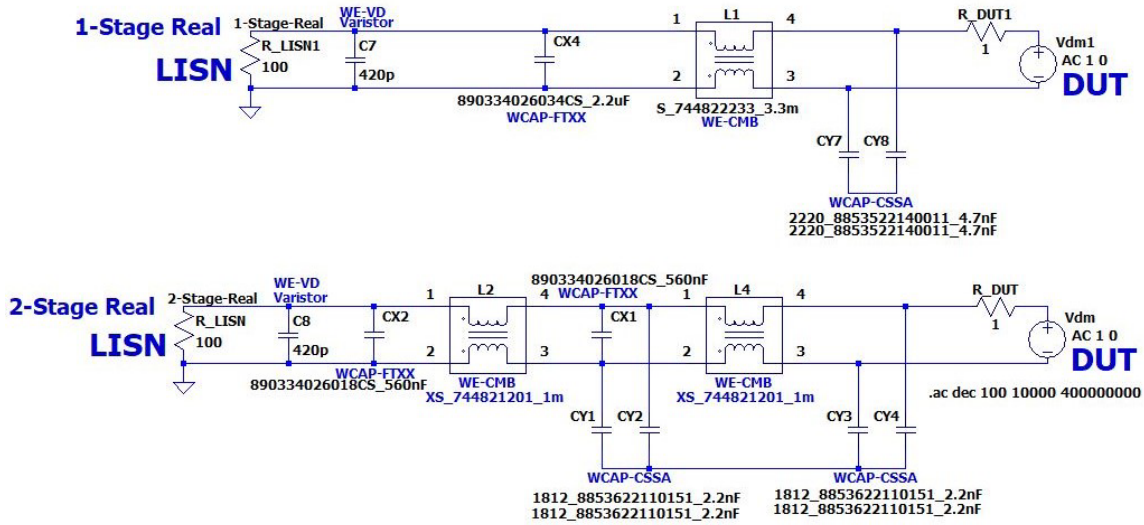

*Figure 16: LTspice circuit diagram for the simulation of **DM** insertion loss with Würth Elektronik LTspice models.*

The superior filtering effect of the two-stage filter versus the single-stage filter can also be seen in DM (Figure 18) above 350 kHz.

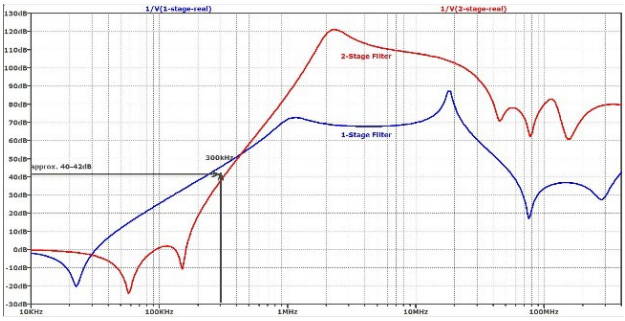

*Figure 18: LTspice simulation of **DM** insertion loss, 10 kHz to 400 MHz; blue = single- stage filter; red = two- stage filter.*

06. COMPARATIVE MEASUREMENTS IN THE EMC LAB

In order to ultimately verify both the calculation and the simulation, the conducted and radiated emission is measured in the EMC Lab at the Würth Elektronik Hightech Innovation Center in Munich. Figure 19 and Figure 23 show the measurement setups and Figure 20 to Figure 22 and Figure 24 to Figure 26 the measurement results.

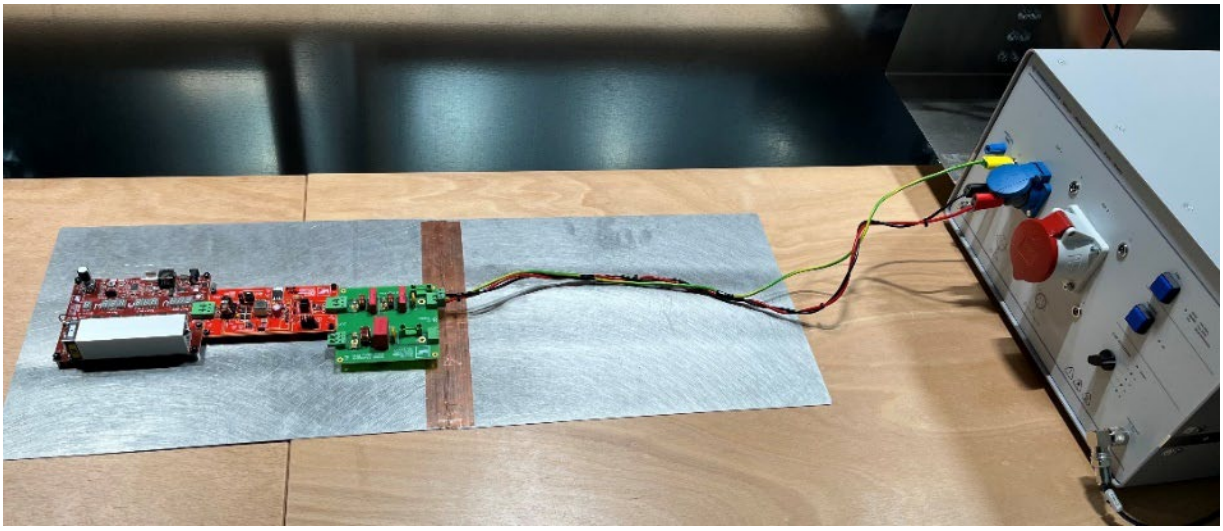

Figure 19: Measurement setup for conducted interference voltage measurement, 150 kHz to 30 MHz; (filter, flyback, elec. load).

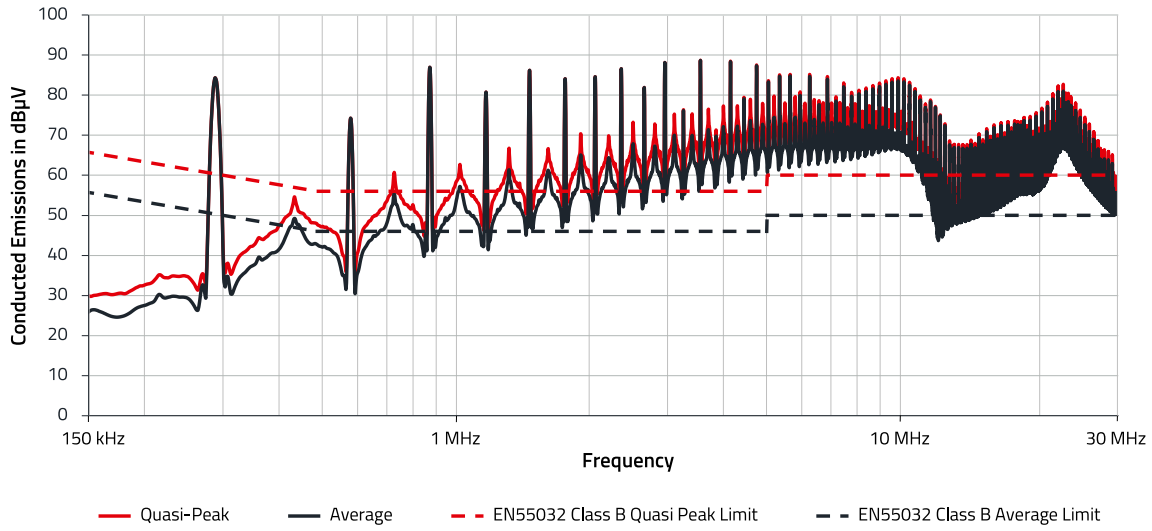

Figure 20: Combined CM and DM measurement of the interference voltage without filter; amplitude of the switching frequency at 300 kHz: 84 dBµV; corresponds almost exactly to the result of the precompliance measurement with the oscilloscope+FFT.

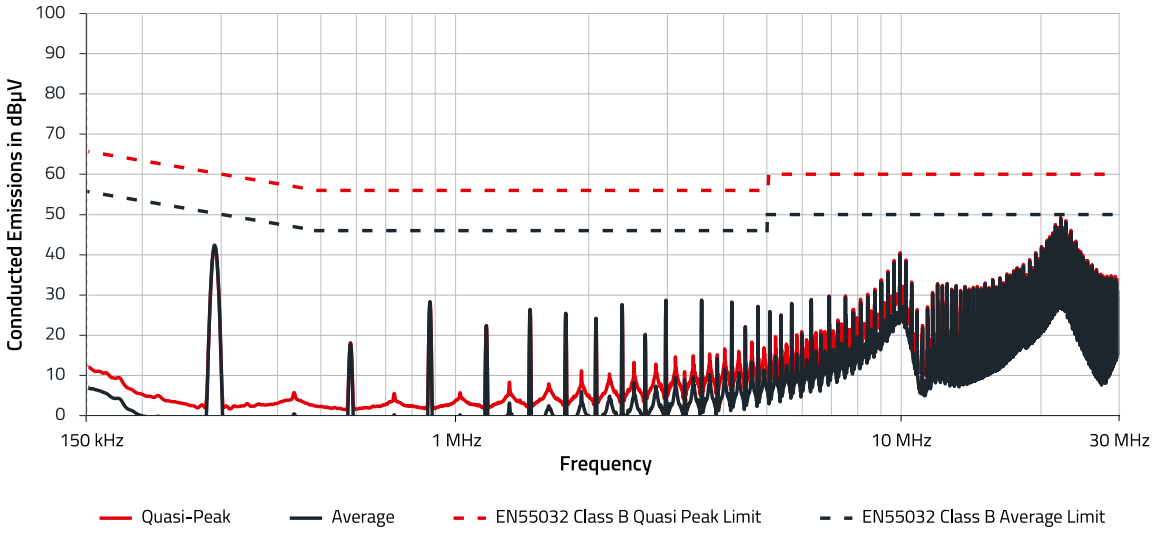

Figure 21: Combined CM and DM measurement of single-stage filter; amplitude of switching frequency at 300 kHz: 43 dBµV (corresponds to 41 dB attenuation).

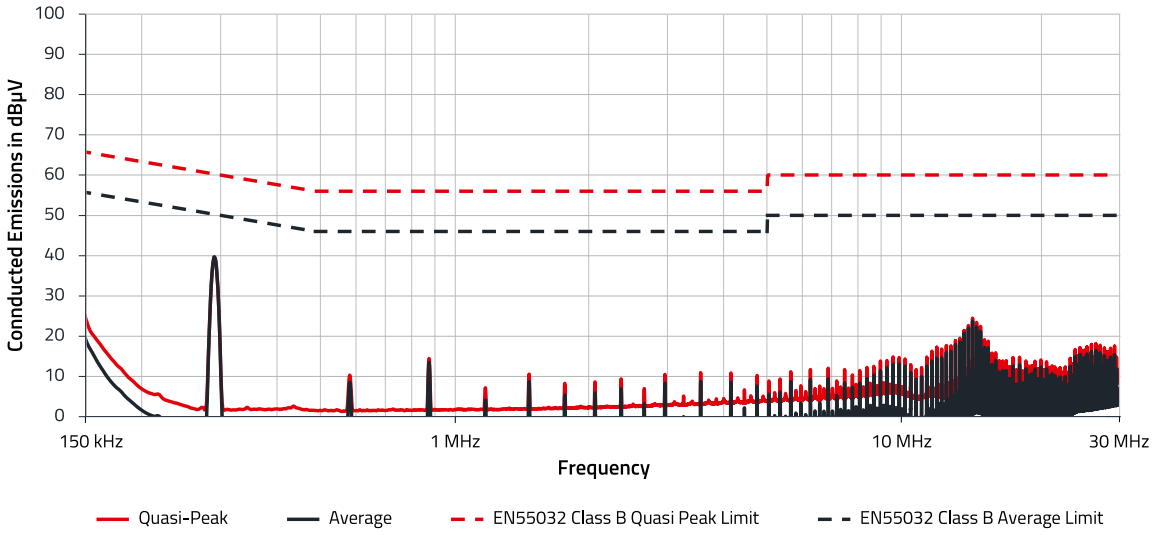

Figure 22: Combined CM and DM measurement of two-stage filter; amplitude of switching frequency at 300 kHz: 39 dBµV (corresponds to 45 dB attenuation).

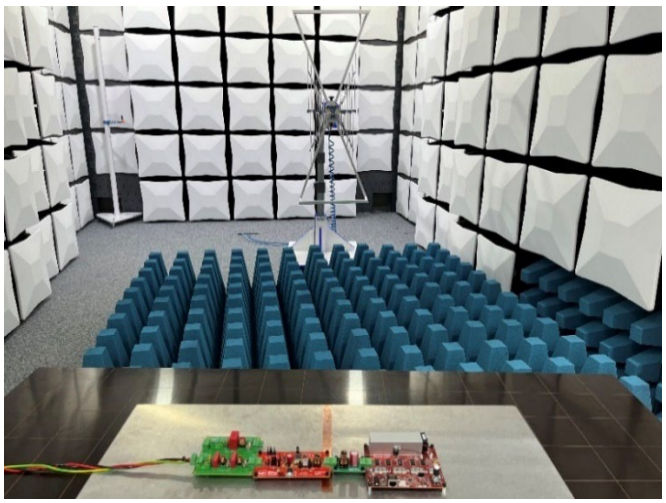

Figure 23: Measurement setup for conducted interference voltage radiated interference emission 30 MHz to 1 GHz; (filter, flyback, elec. load).

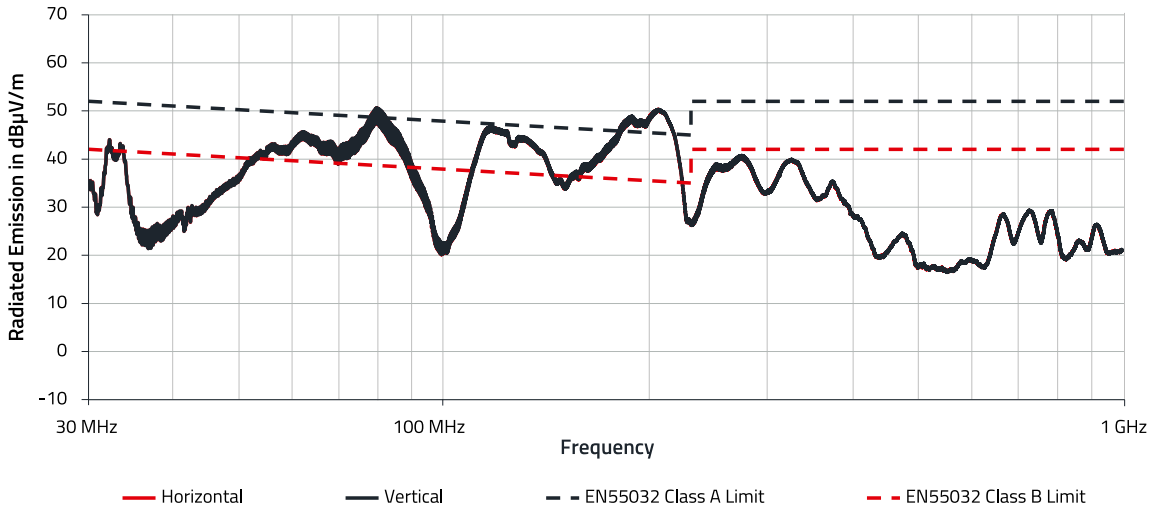

Figure 24: Radiated emission, 30 MHz to 1 GHz without filter.

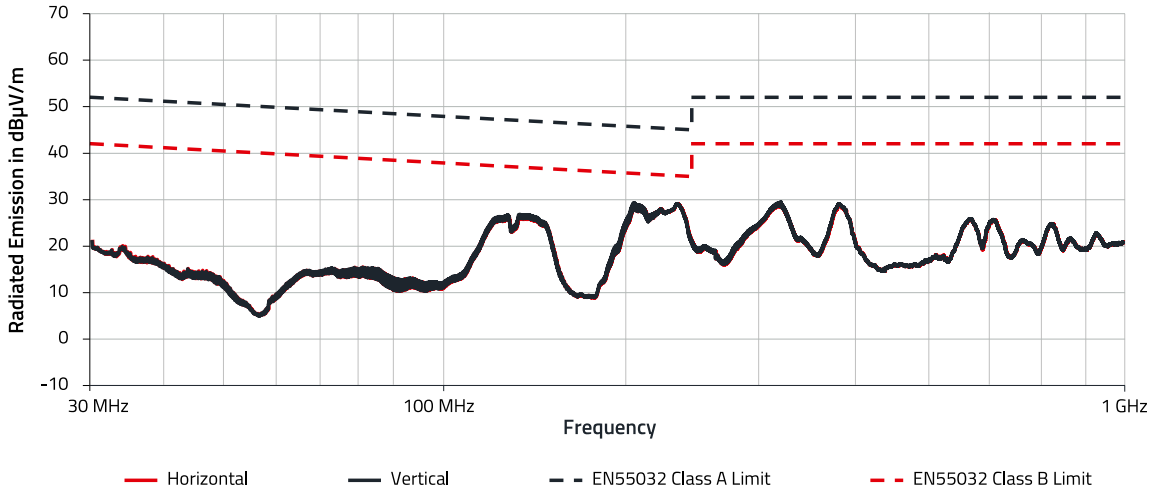

Figure 25: Radiated emission, 30 MHz to 1 GHz single-stage filter.

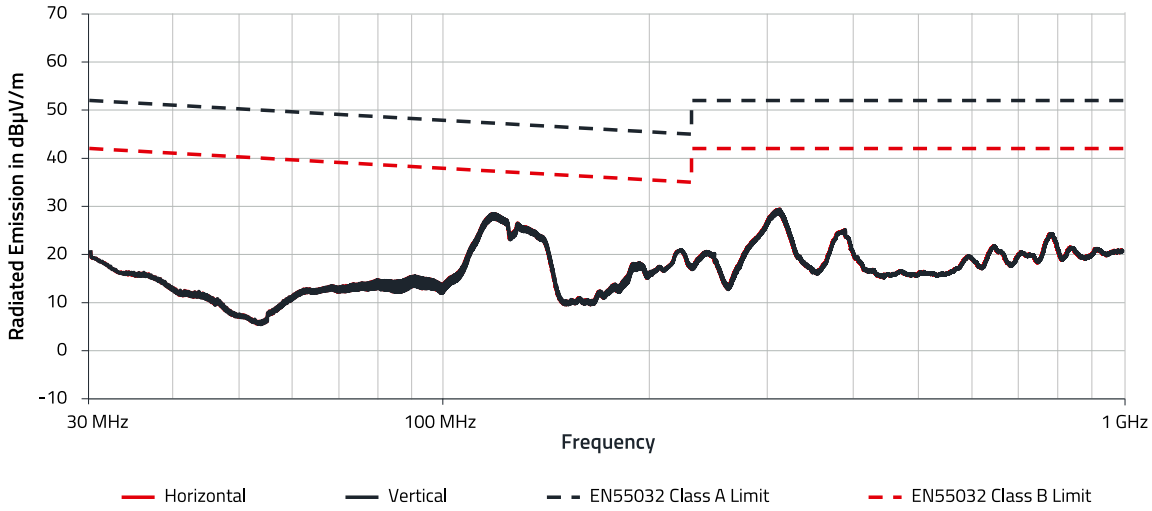

Figure 26: Radiated emission, 30 MHz to 1 GHz two-stage filter.

The two-stage filter achieves a significant reduction in the emitted field strength up to 10 dBµV / m for frequencies above 150 MHz.

Both filter variants produce almost exactly the same attenuation values at the switching frequency, as from the calculation and simulation. It may also be seen here, that the two-stage filter works up to 30 dBµV better in the higher frequency range. With the single-stage filter, there is less than 10 dB clearance to the AV limit at 21 MHz.

Possible causes of deviations between calculation, simulation and practice:

- Inductances of the cables
- Inaccuracies in the simulation model
- Tolerance of inductive and capacitive components
- Saturation of the common mode choke due to excessive CM
- Parasitic inductance of the PCB
- Direct coupling into the filter due to electric and magnetic fields in the vicinity of the components.

07. DIMENSIONING OF THE VARISTOR BETWEEN L AND N

The following design assumes the 'worst case' for the varistor. This is the case at 2 Ω surge generator output impedance, as the highest current can flow through the varistor in this case. The 8 / 20 µs current curve that the generator can drive in a short circuit serves as the basis for the calculation. The schematic test setup is shown in Figure 27.

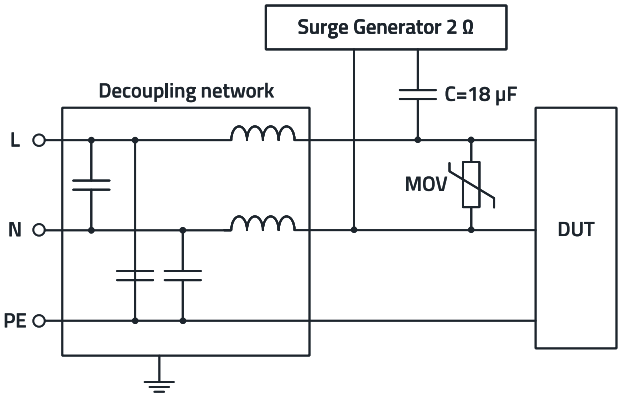

Figure 27: Surge test in the schematic test setup according to IEC 61000-4-5.

The energy contained in the pulse is determined as follows:

$$W_V = \int_0^T I_V(t) \cdot V_V(t)\,dt \sim \hat{I}_V \cdot \hat{V}_V \cdot t_{eq} \qquad (19)$$

Whereby:

T: Time period under analysis

$I_v(t)$ and $V_v(t)$: current and voltage as a function of time

A conservative approximation of the integral is carried out according to Figure 28 with the current and voltage peak values over the time period t_{eq} in an energy-equivalent rectangular pulse.

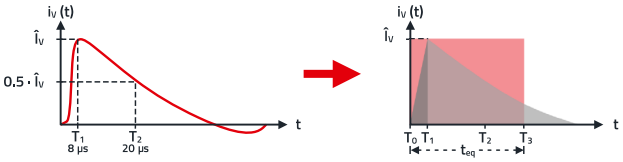

Figure 28: Surge generator short-circuit current curve (8 / 20 µs pulse).

Here the pulse duration t_{eq} is calculated from two time intervals $t_{eq,1}$ and $t_{eq,2}$ as follows:

Linear rise:

$$t_{eq,1} = 0.5 \cdot T_1 \qquad (20)$$

Exponential fall:

$$t_{eq,2} = 1.43 \cdot (T_2 - T_1) \qquad (21)$$

Combined:

$$t_{eq} = t_{eq,1} + t_{eq,2} \qquad (22)$$

This results in an equivalent pulse duration of 21.16 µs for an 8 / 20 µs surge pulse.

Example:

- An industrial application that can withstand max. 1 kV without damage (typical value for bridge rectifiers)
- Surge test with 2 kV (V_G) and 2 Ω (Z_G) generator output impedance between the outer conductors L and N
- Line voltage 230 V_{RMS} (V_{GRID})

Selection of the suitable working voltage (V_{RMS}) of the varistor so it doesn't switch to the conductive state under normal conditions:

$$V_{RMS} > V_{GRID} + Tolerance_{GRID} \qquad (23)$$

$$V_{RMS} > 230\ V_{RMS} + 10\%$$

$$V_{RMS} = 230\ V \cdot 1.1 = 253\ V_{RMS}$$

The next suitable varistor is a type with 300 V_{RMS} (alternatively 275 V_{RMS}) operating voltage.

Experience shows that as far as the power loss P_{DISS} and energy absorption capacity W_{max} is concerned, this varistor must have a diameter of at least 14 mm.

The WE - VD 300 V_{RMS} 820543011 (alternative 275 V_{RMS} 820542711) disc varistor with the electrical properties shown in Figure 29 is therefore selected for this example.

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
AC Operating Voltage	V_{RMS}		300	V	max.
DC Operating Voltage	V_{DC}		385	V	max.
Clamping Voltage	V_{Clamp}	50 A @ 8/20 µs	775	V	max.
(Reverse) Peak Pulse Current	I_{Peak}	8/20 µs	4500	A	max.
Power Dissipation	P_{Diss}		0.6	W	max.
Energy Absorption	W_{max}	10/1000 µs	140	J	max.
Nominal Discharge Current	I_n		3	kA	max.
Measured Limiting Voltage	V_{ML}		1200	V	max.
(Reverse) Breakdown Voltage	V_{BR}	1 mA	470	V	±10%
(Channel) Input Capacitance	C_{Ch}	1 kHz	420	pF	typ.

Figure 29: Data sheet excerpt: Electrical properties WE - VD 820543011; the 300 V_{RMS} operating voltage is already specified with the max. tolerance.

A max. clamping voltage (V_{CLAMP}) of 775 V is specified in the data sheet. This relates to a 50 A surge pulse. However, the current through the varistor is many times higher in the real surge test. The worst case is assumed and the maximum clamping voltage that occurs is determined as follows. This must not exceed the reverse voltage of the semiconductors to be protected.

The first step is to determine the maximum current through the varistor. The calculation is carried out with the maximum clamping voltage (V_{CLAMP_max}) at the short-circuit current (I_G) of the surge generator. To determine V_{CLAMP_max}, the V / I characteristic curve (incl. + 10% tol.) for the component is required.

This can be displayed in REDEXPERT as shown in Figure 30; the values for the short-circuit current (I_G) can be found using the cursor.

For the worst case, the peak value (230 V × 1.41 = 325 V) of the line voltage must also be added to the generator voltage (V_G).

$$I_G = \frac{V_G + V_{GRID}}{Z_G} = \frac{2\ kV + 325\ V}{2\ \Omega} = 1163\ A \qquad (24)$$

The maximum clamping voltage at 1163 A can be read from the diagram or from the product table in REDEXPERT:

$$V_{CLAMP\_max} \rightarrow 1.02\ kV$$

The actual expected varistor current (I_{C1}) can now be further approximated to:

$$I_{C1} = \frac{V_G + V_{GRID} - V_{CLAMP_{max}}}{Z_G} \qquad (25)$$

$$I_{C1} = \frac{2\ kV + 325\ V - 1.02\ kV}{2\ \Omega} = 653\ A$$

The next step is to determine the actual max. clamping voltage using the V / I curve in Figure 31 for current I_{C1}.

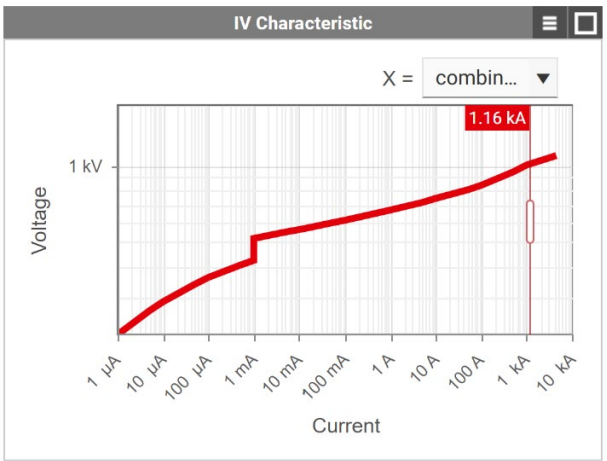

Figure 30: REDEXPERT V / I characteristic curve for the WE - VD disc varistor 820543011, + 10% tolerance at 1163 A. *The desired tolerance can be selected using the drop-down tile at the top right.*

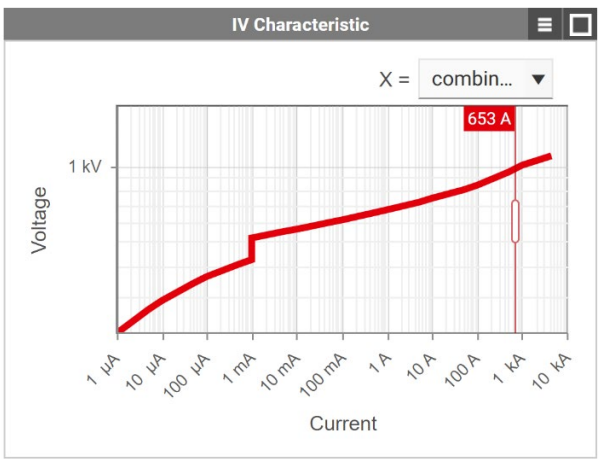

Figure 31: REDEXPERT V / I characteristic curve for the WE - VD disc varistor 820543011, + 10% tolerance at 653 A. The desired tolerance can be selected using the drop-down tile at the top right.

The clamping voltage at 653 A can also be read here from the diagram or from the product table in REDEXPERT:

$$V_{CLAMP} \rightarrow 971\ V$$

The requirement of max. 1 kV from the system specification is therefore complied with. The graph is then set in REDEXPERT to 'min' tolerance
(Figure 32) and the minimum possible clamping voltage V_{CLAMP_min} is read off for I_{C1} = 653 A.

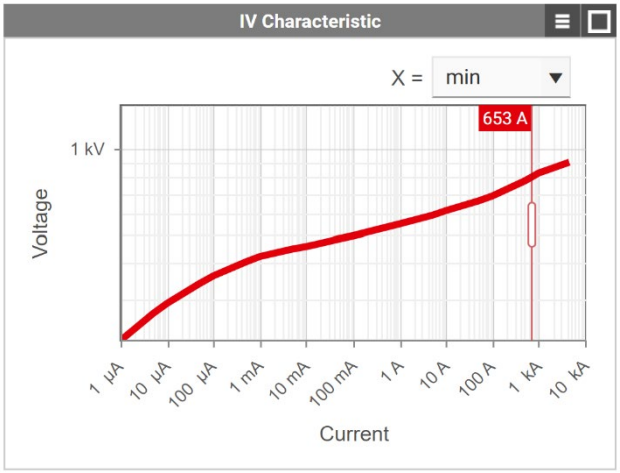

Figure 32: REDEXPERT V / I characteristic curve for the WE - VD disc varistor 820543011, - 10% tolerance at 653 A. The desired tolerance can be selected using the drop-down tile at the top right.

This is required to determine the maximum possible current (I_{C_max}) through the varistor.

$$V_{CLAMP\_min} \rightarrow 794\ V$$

$$I_{C\_max} = \frac{V_G + V_{GRID} - V_{CLAMP\_min}}{Z_G} \qquad (26)$$

$$I_{C\_max} = \frac{2\ kV + 325\ V - 794\ kV}{2\ \Omega} = 766\ A$$

Now check how many 766 A current pulses the selected varistor can withstand in relation to its lifetime. It is important that the varistor does not fail during the surge test with a total of 40 pulses (5 × positive, 5 × negative, at 90 °, 180 °, 270 ° phase angle). There is a graph in the data sheet (Figure 33) in the form of a set of curves that shows the lifetime of the varistor as a function of the number of pulses and the pulse duration at various maximum currents flowing through the varistor.

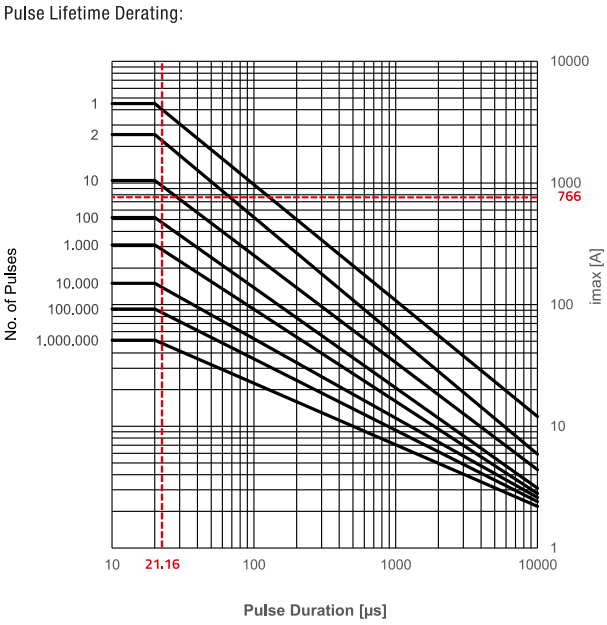

Figure 33: Lifetime derating over current, pulse length & number of pulses. Using a rectangular equivalent of 21.16 µs and a current of 766 A, the varistor safely withstands approx. 50 pulses. A total of 40 pulse loads occurs during the surge test in accordance with IEC / EN 61000-4-5.

Although a 'worst case' analysis is carried out here, the conventional varistor may still not be sufficient depending on the specification. In this case, a 14 mm High Surge type, WE - VD 820443011E (alternatively 275 V_{RMS} 820442711E High Surge) should be used, which is specified for 500 load pulses with 21.16 µs pulse length at a 766 A pulse current.

Next, the maximum energy emitted in the varistor is checked:

$$W_{max} = I_{C\_max} \cdot V_{CLAMP\_min} \cdot t_{Pulse} \qquad (27)$$

$$W_{max} = 766\ A \cdot 794\ V \cdot 21.16\ \mu s$$

$$W_{max} = 12.9\ Ws$$

The data sheet specifies a maximum possible energy absorption of 140 Ws (joules).

It is then investigated whether the varistor has enough time to cool down between surge pulses (T_{cool}). IEC 61000-4-5 specifies that a pulse should be sent to the DUT every 60 seconds.

A maximum power loss P_{DISS} of 0.6 W can be taken from the data sheet.

$$T_{cool} > \frac{W_{max}}{P_{DISS}} = \frac{12.9\ Ws}{0.6\ W} = 21.5\ s \qquad (28)$$

The selected varistor needs less than 22 seconds to cool down and is therefore ideally suited for use in the application.

If a higher operating voltage or energy absorption capacity is required, e.g., for 3-phase applications, the WE - VD 820524611 varistor with a 20 mm disc diameter can be selected.

The entire worst-case analysis applies when the positive surge pulse reaches a 90° phase angle and the negative pulse 270°. For all other phase angles, the load for the varistor is significantly lower.

The reader will find a real measurement of the clamping voltage & clamping current in the Appendix.

08. CALCULATION OF THE LEAKAGE CURRENT THROUGH Y-CAPACITORS

Y-capacitors are an effective instrument for reducing common-mode emissions. The greater the capacitance selected, usually the greater the reduction in EMC interference levels. However, the leakage currents to PE also increase with rising capacitance. Depending on the industrial standard and protection class, leakage currents from a few µA (e.g., medical technology) to many mA (e.g., permanently installed industrial systems) are permitted. In practice, a limit on the values for common applications with protective conductors is 3.5 mA. Figure 34 shows a simplified block diagram of a line filter with Y- and X-capacitors.

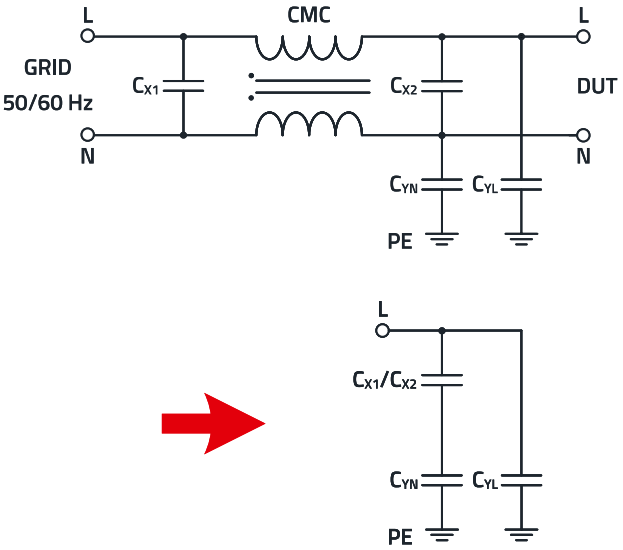

Figure 34: Simplified block diagram of a typical line filter; if one or more X-capacitors are used, they are connected in series with one of the two Y-capacitors. But this only applies in the event of a fault if PE or N are not connected. Normally, these are at almost the same electrical potential.

In addition, the level of the leakage current depends on the line voltage V_{GRID}, the line frequency f_{GRID}, and the X-capacitors.

$$I_{LEAK} = V_{GRID} \cdot 2\pi \cdot f_{GRID} \cdot \left(C_{YL} + \frac{C_{XG} \cdot C_{YN}}{C_{XG} + C_{YN}}\right) \quad (29)$$

$$C_{XG} = C_{X1} + C_{X2} \quad (30)$$

Example:

C_{X1}, C_{X2} = each 1 µF; C_{Y1}, C_{Y2} = each 5.6 nF; 230 V / 50 Hz

Worst case tolerance: Line voltage + 10%; capacitance + 20%

$$I_{Leak} = 253\ V \cdot 2\pi \cdot 50\ Hz \cdot \left(5.6\ nF + \frac{2.4\ \mu F \cdot 5.6\ nF}{2.4\ \mu F + 5.6\ nF}\right) = 0.89\ mA \quad (31)$$

09. CALCULATION OF THE DISCHARGE RESISTANCE FOR X-CAPACITORS

A further safety requirement (IEC 60950, 60335, 62368) is that the touchable voltage (V_{GRID}) must drop below 60 V ($V_{discharge}$) for plug-in devices within one second of being disconnected from the power line. To ensure this, the capacitances between the outer conductors must be discharged by means of resistance ($R_{discharge}$).

Figure 35 shows a simplified block diagram of a line filter with an additional discharge resistor and a varistor.

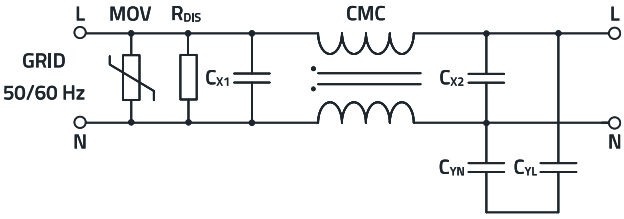

Figure 35: Simplified block diagram of a typical line filter with a discharge resistor.

The capacitances essentially include the X-capacitors, as these predominate in terms of capacitance values. However, the capacitance of the varistor (Metal Oxide Varistor, MOV) and the Y-capacitors connected in series as far as the outer conductors are concerned, must also be considered in a worst-case calculation. The worst-case tolerance of the capacitors (+20%) and the supply voltage (+10%) must also be taken into account.

The larger the total capacitance (C_{tot}) the smaller the resistance must be in order to discharge the capacities within the required time ($t_{discharge}$).

$$C_{tot} = C_{X1} + C_{X2} + C_{ParaMOV} + \left(\frac{1}{\frac{1}{C_{YL}} + \frac{1}{C_{YN}}}\right) \quad (32)$$

$$V_{discharge} = V_{GRID} \cdot e^{-\left(\frac{t_{discharge}}{R_{discharge} \cdot C_{tot}}\right)} \quad (33)$$

$$R_{discharge} < \frac{\left(-\ln\left(\frac{V_{discharge}}{V_{GRID}}\right)\right)^{-1}}{t_{discharge}} \cdot \frac{1}{C_{tot}} \quad (34)$$

$$P_v(\text{Discharge Resistor}) = \frac{V_{GRID\_RMS}^2}{R_{discharge}} \quad (35)$$

Example:

C_{tot} = 2.1 µF + 20% / V_{GRID} = 230 V + 10%

$$R_{discharge} < \frac{\left(-\ln\left(\frac{60\ V}{253\ V}\right)\right)^{-1}}{1\ s} \cdot \frac{1}{2.52\ \mu F} = 256\ k\Omega$$

→ 240 kΩ selected

$$P_v(\text{Discharge Resistor}) = \frac{(253\ V)^2}{240\ k\Omega}$$

P_v(Discharge Resistor) = 267 mW

In addition, both the dielectric strength as well as the creepage and clearance distance must be taken into account for the discharge resistor.

10. LINE FILTER LAYOUT & COMPONENT INSTRUCTIONS

There are two basic aspects to consider in the layout. The first is electrical safety and the second is parasitic effects, which have an impact on insertion loss, i.e., filter efficiency. To ensure electrical safety, different creepage and clearance distances must be maintained depending on the operating voltage, contamination class, material and overvoltage category. In addition, only components may be used that meet the current safety requirements, e.g., UL or VDE.

To ensure optimum filter effectiveness, the following points must be observed in the design and layout of the filter:

- The connection to PE, i.e., the reference_GND of the Y2-capacitors, should be as low-inductance as possible. Only in this way can the Y2-capacitors achieve a high filter effect. Figure 36 shows such a connection with WA - SMST steel spacer.

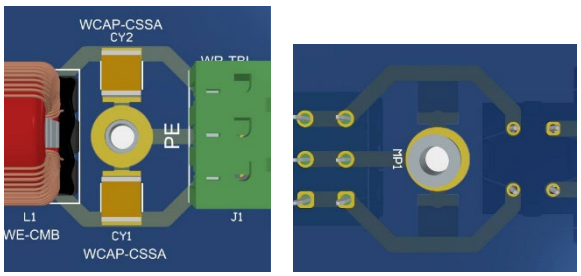

Figure 36: TOP & BOTTOM view of the Y2 - capacitors incl. low-inductance PE connection using WA - SMST SMT spacer bolts.

- There must be no copper filled areas below common mode chokes (Figure 37). These would increase the parasitic coupling capacitance from input to output and therefore worsen the insertion loss in the higher frequency range.

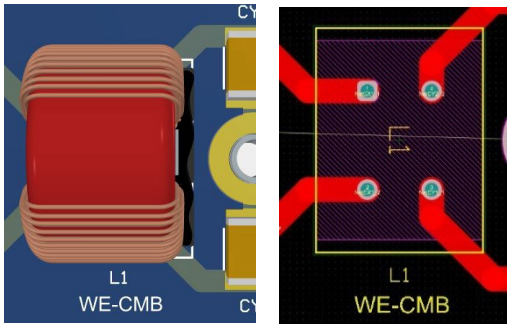

Figure 37: 3D & 2D view of the connection of the WE - CMB common mode choke used.

- Whenever possible, no stub lines should be routed to the connection pads of the components. As can be seen in Figure 38, the conductor tracks should always be routed directly through the component pads in order to reduce the parasitic connection inductance as much as possible.

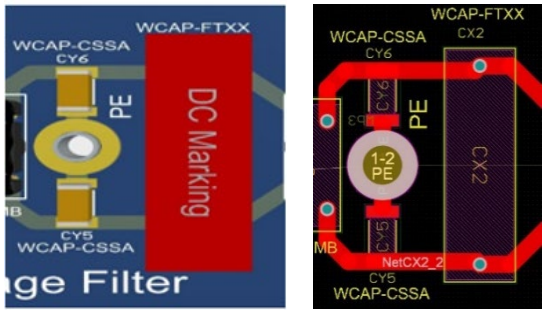

Figure 38: 3D & 2D view of the connection of the X2 / Y2 capacitors used.

- The filter effect of both the inductors and capacitors can be compromised by near-field coupling of H and E fields. Therefore, it is advisable to place the filter components at a carefully selected distance from each other as well as away from sources of interference (Figure 39).

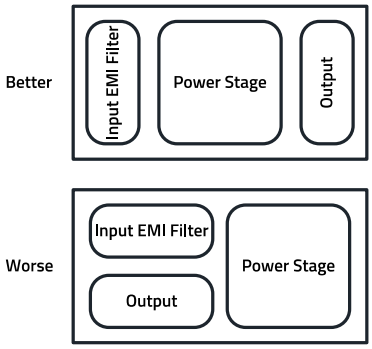

Figure 39: Simplified representation of the filter arrangement.

11. CORE MATERIALS FOR COMMON MODE CHOKES (CMCS)

Würth Elektronik has three different core materials available for common mode chokes:

- Manganese-zinc (MnZn)
- Nanocrystalline (NC)
- Nickel-zinc (NiZn)

As can be seen in Figure 40, the widest bandwidth material is nanocrystalline. Manganese-zinc offers high insertion loss, especially between 50 kHz and 5 MHz. Nickel-zinc works optimally if the filter is to have a higher insertion loss from 5 MHz to 500 MHz.

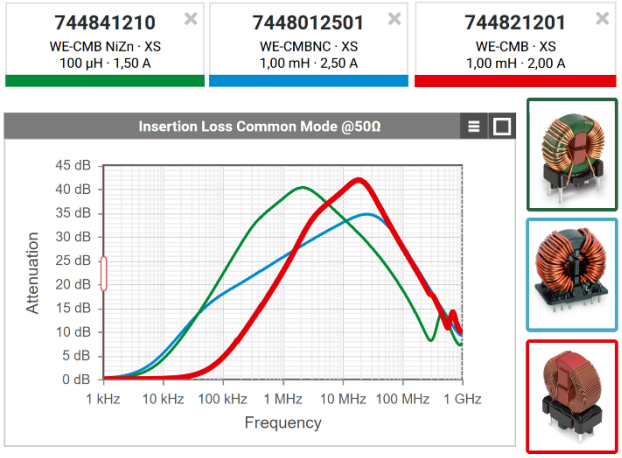

Figure 40: Insertion loss (common mode) measured for three common mode chokes with different core materials from 1 kHz to 1 GHz.

In the previous sections, the filter is designed on the basis of the nominal inductance. However, this consideration only works if this inductance value is stable around the switching frequency (or the frequency for which the filter is designed) and has not already fallen sharply. The nominal inductance is often measured at 10 kHz, but the inductance is a function of frequency.

Figure 41 shows the impedance curves of two common mode chokes with the same nominal inductance (1 mH) and same package (XS).

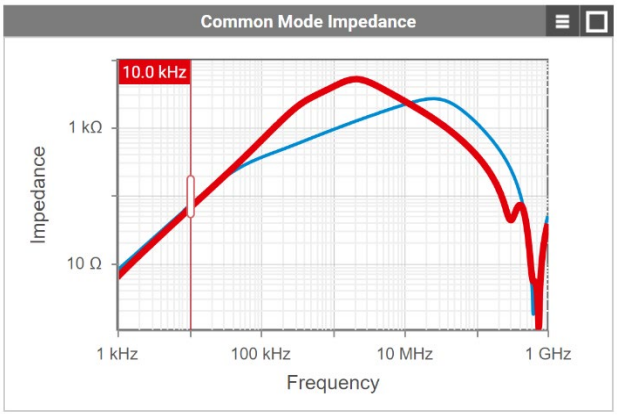

Figure 41: Common mode impedance over the frequency of a 1 mH manganese-zinc (744821201) and a 1 mH nanocrystalline (7448012501) common mode choke (REDEXPERT).

It can be seen that at 10 kHz, where the nominal inductance is measured, the curves are almost congruent. Above approx. 50 kHz, the impedance curve of the nanocrystalline choke starts to flatten out noticeably due to the frequency-dependent permeability of the core.

In the case of the manganese-zinc choke, a change occurs above approx. 300 kHz. If the impedance at 1 MHz is compared and calculated back to the resulting common mode inductance, the following values arise:

- 1 mH MnZn 744821201 at 1 MHz: Z = 3.91 kΩ, corresponding to L = **0.62 mH**
- 1 mH NC 7448012501 at 1 MHz: Z = 0.915 kΩ, corresponding to L = **0.146 mH**

It it is true to say that the nominal inductance is not always the appropriate starting value for the filter design, depending on the frequency and core material. A better approach is to use REDEXPERT to calculate the common-mode impedance at the desired frequency (e.g., switching frequency). Care should also be taken to ensure that the choke has sufficient distance between the natural resonant frequency and the desired frequency. Above the resonant frequency, the impedance curve and therefore the insertion loss starts to fall.

Moreover, the developer should keep the temperature dependence of the common-mode inductance (impedance) in mind during design. This is shown in Figure 42.

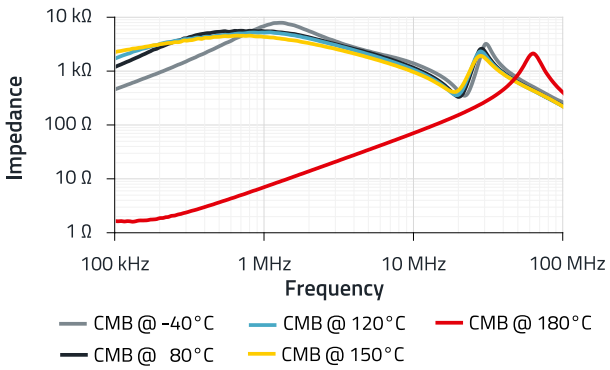

Figure 42: Measured common mode impedance of a manganese-zinc (WE - CMB) common mode choke at different temperatures in °C.

At very low temperatures, the permeability of the core and therefore the inductance of the coil drops significantly. On the other hand, if the Curie point of the core is exceeded (at 180 °C in the graph), the core material loses all its magnetic properties. Then there is only the impedance of the winding (air coil).

Figure 43 shows that nanocrystalline cores do not show this temperature dependence.

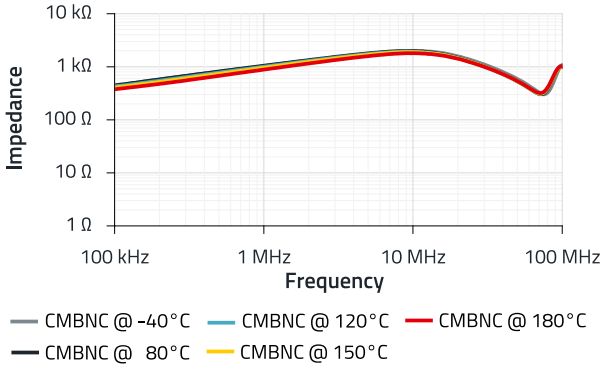

Figure 43: Measured common-mode impedance of a nanocrystalline (WE - CMBNC) CMC at different temperatures in °C.

This property, combined with the very broadband impedance available, makes them the first choice in many applications.

If a filter with a CMC does not work as desired and/or it becomes hotter during operation than the rated current would suggest, the core may be saturated due to excessive common mode current.

Figure 44 shows that all CMCs, regardless of the core material, display a pronounced saturation with increasing common-mode current.

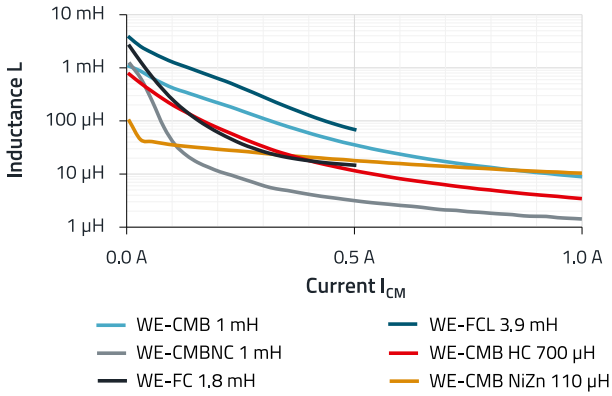

Figure 44: Measured common-mode inductance of different CMCs with different core materials against the common-mode current.

This is due to the absence of an air gap in the core, which prevents premature saturation, as seen for example in classic storage chokes. In practice, common mode current is generally below 10 mA and is therefore relatively uncritical. High common-mode current occurs, for example, in motor-inverter applications. Here there is often high capacitive coupling to PE, which means that a high common-mode current can circulate and thus drive a CMC into saturation.

12. WE-CLFS LINE FILTERS

If you don't want to set up a discrete filter, an integrated filter from the WE-CLFS series, as shown in Figure 45, offers an alternative.

Figure 45: WE-CLFS line filters certified to IEC/EN/UL 60939-2.

These contain all the components required for a line filter (apart from varistors). single- and two-stage versions are available. There are also variants without Y-capacitors for applications in which no leakage current is permitted (e.g., medical technology). The filters cover a rated current range from 1.5 to 20 A. In order for these integrated filters to work properly, the metal package must have a solid, low impedance connection to PE/chassis. In addition, the input and output connection cables must be routed a sufficient distance away from each other to prevent unwanted coupling.

13. SUMMARY

It is shown how the developer can successfully design an AC line filter using simple mathematics and common measurement technology. The primary aim is to dimension the filter correctly in terms of insertion loss in order to avoid unnecessary costs and keep the filter design as compact as possible. The advantage of a two-stage filter over a single-stage filter was also proven. Würth Elektronik offers an extensive portfolio of passive and electromechanical components to build a complete line filter. In Appendix to this application note, the reader will find further information on the topics already described.

A Appendix

A.1 Parts list

Index	Description	Value	Package size	Art. no.
CY1/2	Y-Capacitor	4,7 nF / 250 V	2220	8853522140011
CY3/4/5/6	Y-Capacitor	2.2 nF / 250 V	1812	8853622110151
CX1	X-Capacitor	2.2 µF / 310 V	THT	890334027021CS
CX2/3	X-Capacitor	560 nF / 310 V	THT	890334026018CS
L1	CMC	3.3 mH / 250 V	S	744822233
L2/3	CMC	1 mH / 250 V	XS	744821201
VAR1/2	Varistor	300 V / 14 mm	THT	820443011E
MP1-5	SMT Bolt	OD 6 mm Hole 3.3 mm	SMT	9774050960R
XF1/2	Fuse Holder	250 V_{AC} 6.3 / 20 A	5 × 20 mm	696106003002
XF1/3	Clipcover Fuse		5 × 20 mm	696122003001
J1/3	Terminal Block	300 V_{AC} 20 A	5.08 mm	691309510003
J2/4	Terminal Block	300 V_{AC} 20 A	5.08 mm	691313510003

A.2 Measurement and Calculation for a two-stage filter

Surge Test: IEC/EN 61000-4-5

Conducted emission test: IEC/EN 55032/55011

Radiated emission test: IEC/EN 55032/55011

Two-stage filter component values that differ greatly:

Two-stage Calculation:

When the values of the filter components differ greatly (DM example) such as when the size of the inductors are different, then there are two pairs of poles: High & Low frequency pole.

In this example L1 has the bigger inductance and C1 the bigger capacitance:

$$\Delta s = \left[1 + \frac{s}{\omega_L \cdot Q_L} + \frac{s^2}{\omega_L{}^2}\right] \cdot \left[1 + \frac{s}{\omega_H \cdot Q_H} + \frac{s^2}{\omega_H{}^2}\right] \tag{36}$$

$$\omega_L = \frac{1}{\sqrt{L_1 \cdot C_p}} \tag{37}$$

$$\rightarrow f_{CL} = \frac{1}{2\pi \cdot \sqrt{L_1 \cdot C_p}}$$

$$C_p = C_1 + C_2 \tag{38}$$

$$\omega_H = \frac{1}{\sqrt{L_2 \cdot C_S}} \tag{39}$$

$$\rightarrow f_{CH} = \frac{1}{2\pi \cdot \sqrt{L_2 \cdot C_S}}$$

$$C_S = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} \tag{40}$$

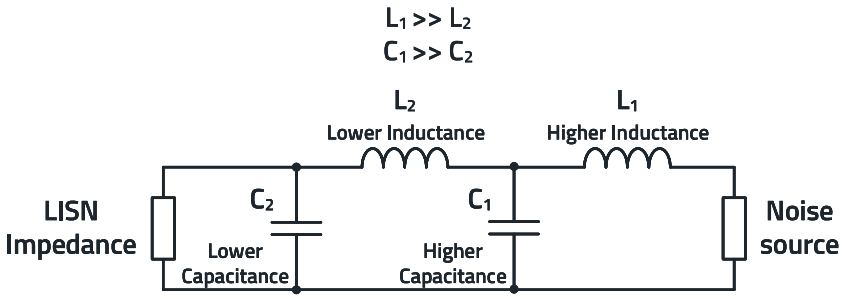

Figure 46: Simplified circuit diagram of a two-stage filter in which the component values differ greatly.

Two-Stage Simulation Example:

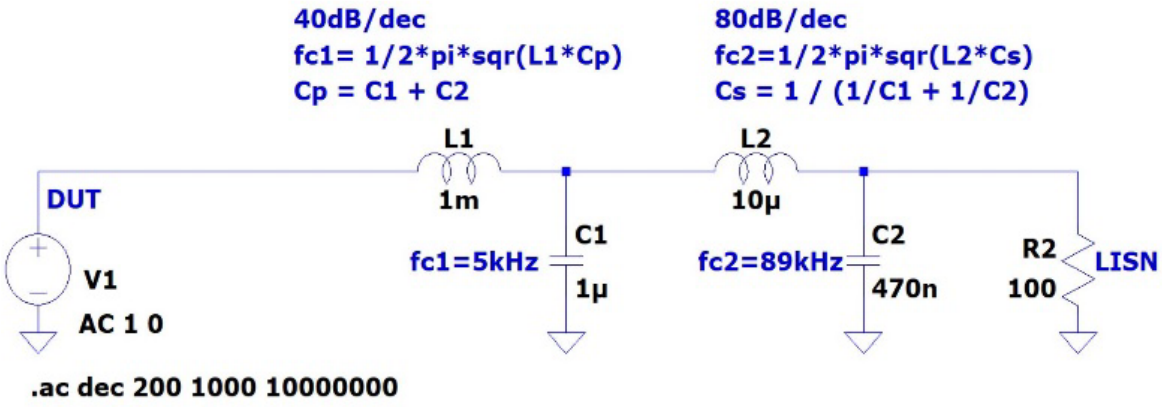

Figure 47: LTspice circuit diagram for simulation Würth Elektronik Spice models.

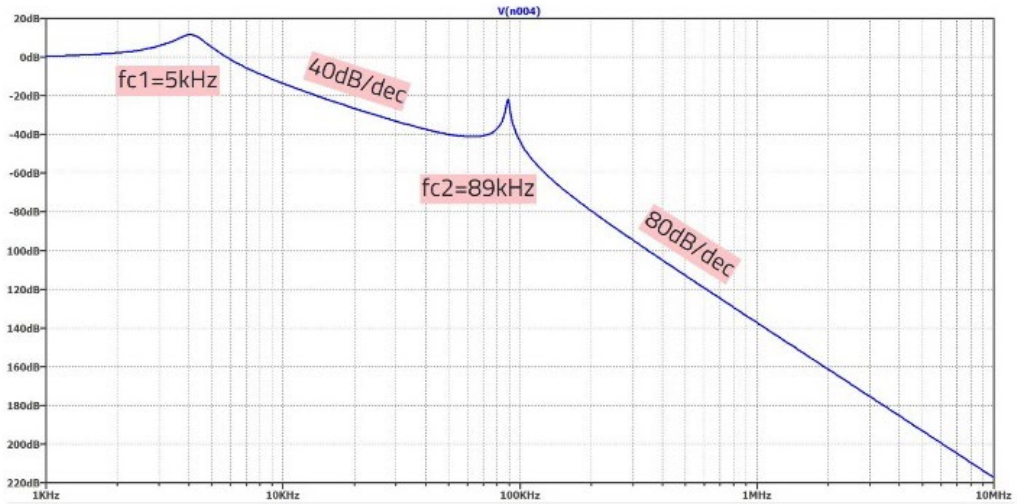

Figure 48: The two-stage filter attenuation behavior.

A.3 Real 2 kV surge test with the calculated varistor 820543011 on a resistive load (light bulb)

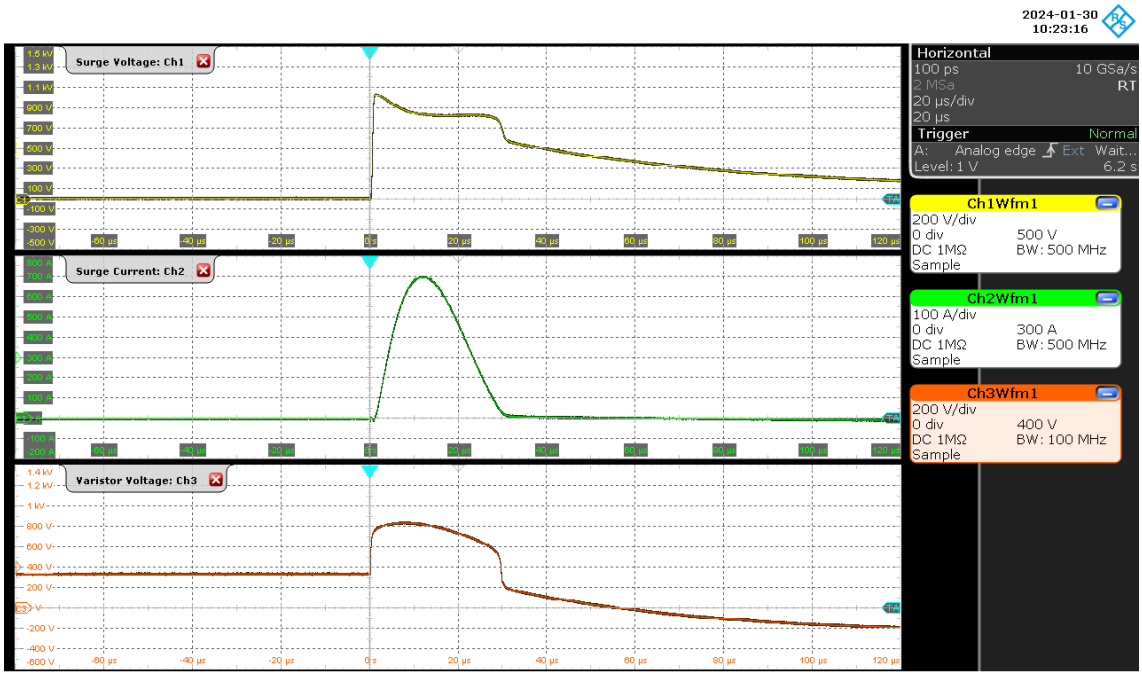

Figure 49: WE-CLFS line filters certified to IEC/EN/UL 60939-2.

Yellow curve: Voltage at the surge generator.

Green curve: Current through varistor = 700 A max.

Red curve: Voltage across varistor = 850 V max.

A.4 References

[1] Trilogy of Magnetics, 5th edition

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