# APPLICATION NOTE

## ANP017 | Designing Buck Converters with Isolated Outputs

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## 1. INTRODUCTION

The DC-DC Buck converter is, in addition to the boost and buck-boost converters, one of the fundamental non-isolated switching power supply topologies. It provides a regulated output voltage which is lower than the converter input voltage. Such 'step-down' voltage conversion is widely required in electronic applications and, especially for input voltages under 80 V, the buck converter is extremely popular thanks to its design simplicity, low component count, high efficiency, well understood dynamic behavior and robust feedback loop compensation methods.

The most common bus voltage levels found in industries like telecom, industrial, automotive or consumer are 48 V, 24 V and 12 V. These voltages need to be stepped down to the bias supply voltages that digital and analog circuitry need to operate (e.g. 5 V, 3.3 V or even down to 0.8 V (FPGA/ASIC core systems)). When galvanic isolation is not required, the buck converter provides a good compromise between performance, size and cost.

Some applications require more than one low-voltage supply rail, and sometimes of opposite polarity with respect to the input supply. Examples are the ±15 V required in some signal conditioning circuits as well as the asymmetrical bipolar voltages like +20 / -5 V used in gate driver systems. In many cases, these output voltage rails must be also galvanically isolated from the input voltage supply circuit. Isolation may be required not only for protecting sensitive low-voltage circuitry or for user safety in high-voltage applications, but also for signal integrity and noise immunity, as it prevents large ground loops and can help improve EMI performance. Examples of such applications are I/O module cards in industrial automation PLC systems (Programmable Logic Controllers), isolated field communication interfaces (e.g. CAN, RS-485, RS-232, etc) as well as high-voltage isolated gate driver systems (e.g. industrial AC-motor drives, solar power inverters, E-mobility traction inverter, etc).

These low-power isolated voltage rails could be obtained with a traditional isolated DC-DC topology, like flyback, push-pull or half-bridge. However, in some target applications, a non-isolated output voltage rail is also used.

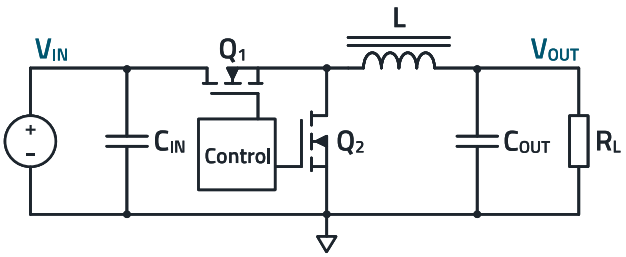


*Figure 1: Synchronous Buck Converter Power Stage*

In such cases, a buck converter (Figure 1) can be used to easily and cost-effectively obtain multiple isolated outputs, while also providing a well-regulated, non-isolated voltage rail. This is achieved by adding separate coupled windings to the power inductor and using a peak rectifier circuit, formed by a diode and a capacitor, on each output (Figure 2).

The topology takes advantage of the fact that, during the off-time of the control transistor ($Q_1$), the well-regulated buck converter output voltage is reflected to any other secondary windings, allowing the isolated outputs to indirectly track the main output voltage, scaled as desired by the corresponding turns-ratio. Since the isolated outputs are only indirectly regulated, it is very important to understand the impact that various parameters will have on the regulation of these isolated rails.

$$L_{S,k} = \left(\frac{N_{S(k)}}{N_P}\right)^2 \cdot L_P$$

$$V_{OS,k} \approx \frac{N_{S(k)}}{N_P} \cdot V_{OP}$$

$N_{S(k)}$: Number of turns of 'k' winding

$N_P$:Number of turns of primary winding

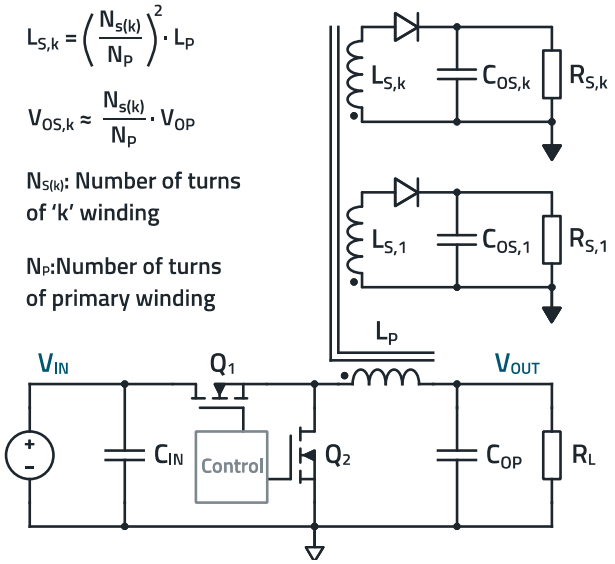


*Figure 2: Buck Converter with Isolated Outputs*

In this application note, the converter operation is explained and important design considerations provided, all supported by SPICE simulation and experimental results. Special attention is given to the voltage regulation of the isolated output rails. In addition, a validated step-by-step design example is also provided as a reference.

NOTE: this topology has also been named as Flybuck™ by Texas Instruments and as Iso-buck™ by former IC manufacturer Maxim Integrated (now part of Analog Devices).

## 2. REVIEW OF SYNCHRONOUS BUCK CONVERTER

Before diving into the analysis of the buck converter with additional isolated outputs, a good understanding of the synchronous buck converter operation is required.

The power stage of the synchronous buck converter is shown in Figure 1, with the electronic switches $Q_1$ and $Q_2$ commonly implemented with MOSFET transistors. Its main waveforms are shown in Figure 4 based on the reference schematic of Figure 3. It is observed that $Q_1$ and $Q_2$ are configured in half-bridge, switching alternately, and thus alternately connecting the input voltage rail and power ground reference to the 'switching' node (SW node). This generates a square-like waveform as a result ($V_{SW}(t)$).

The frequency of $V_{SW}(t)$ equals the converter switching frequency ($F_{SW}$), and its duty cycle (D) equals the duty cycle of $Q_1$, which is given by $Q_1$ conduction time ($t_{ON}$) divided by the switching period ($T_{SW}$):

$$D = \frac{t_{ON}}{T_{SW}} \quad (1)$$

A second-order low-pass LC filter is connected to the SW node at the output stage of the converter. It filters out the fundamental frequency and harmonic components of $V_{SW}(s)$, leaving only the DC average voltage value at the output of the converter, which directly depends on the duty cycle of $V_{SW}(t)$ and the input voltage ($V_{IN}$). The converter output voltage ($V_{OUT}$) can then be set via $Q_1$ duty cycle as:

$$V_{OUT} = D \cdot V_{IN} \quad (2)$$

However, to achieve the above, the cut-off frequency of the LC filter needs to be set lower (recommended 10 times lower) than the switching frequency, as follows:

$$F_{SW} > \frac{10}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \quad (3)$$

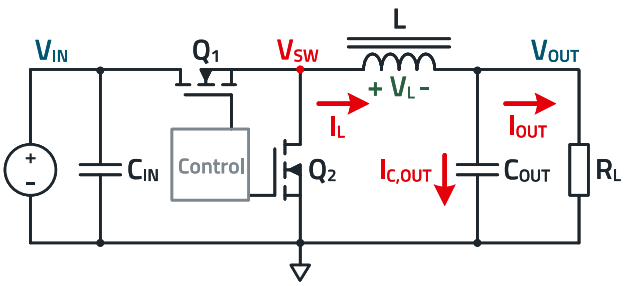


*Figure 3: Reference Schematic Synchronous Buck Power Stage*

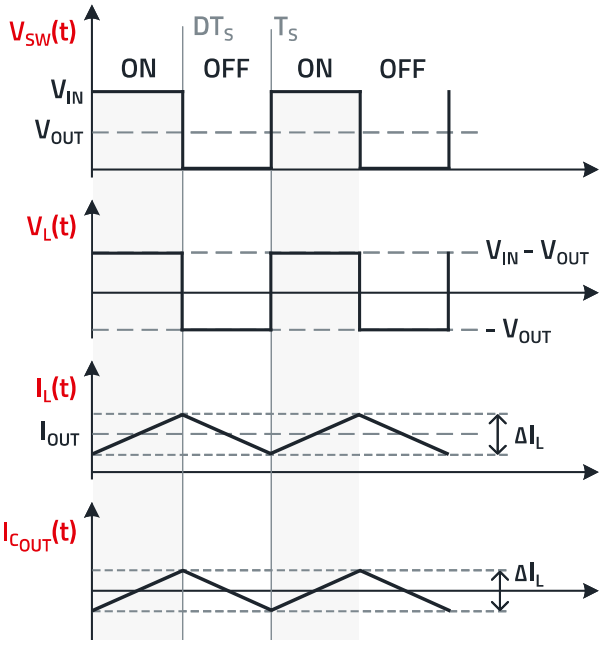


*Figure 4: Main switching waveforms of synchronous buck converter*

It is important to note that, unlike a typical EMI filter, the inductor and capacitor of this LC filter are energy storage components of the buck power stage. Therefore, their values cannot be chosen loosely just to meet the condition set in (3). Here, the inductance (L) must be high enough to limit the peak-to-peak ripple amplitude of the inductor current ($\Delta I_L$), as follows:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{\Delta I_L \cdot F_{SW}} \quad (4)$$

Typically, a peak-to-peak ripple amplitude of 20 - 40% of the maximum output current of the converter is considered as a good trade-off between solution size, cost and efficiency.

Similarly, the output capacitance ($C_{OUT}$) is selected to limit the ripple amplitude of the output voltage ($\Delta V_{OUT}$):

$$C_{OUT} \approx \frac{\Delta I_L}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (5)$$

Note that the above equation (5) considers negligible ESR of the output capacitors (e.g. Multilayer Ceramic type). Maximum acceptable peak-to-peak output voltage ripple depends on the application, but it is typically found in the range of 0.5% to 2% of $V_{OUT}$.

In steady-state operation, there is no net energy stored in the inductances and capacitances of the circuit in a full switching period, giving rise to what is known as 'volt-second compensation' for inductances and 'charge balance' for capacitances.

Equations (4) and (5) can be obtained based on this principle. This simply means that any net energy stored during $Q_1$ on-time in these reactive elements will need to be delivered during $Q_1$ off-time, and vice versa.

Figure 5 and Figure 6 show the equivalent circuit of the buck converter during $Q_1$ on- and off times, respectively.

During the on-time, energy is transferred from the input supply and input capacitor to the inductor (storage) and output load. There is no net energy stored in the output capacitor during this time window, since its average current (and in turn delta charge) is zero (Figure 3).

During the off-time, the input supply and input capacitor are disconnected from the output stage and load. The inductor now supplies the energy previously stored to the load, and the input supply charges the input capacitor.

The output capacitor in the buck converter simply filters the AC ripple of the inductor current, leaving only the DC current to the load.

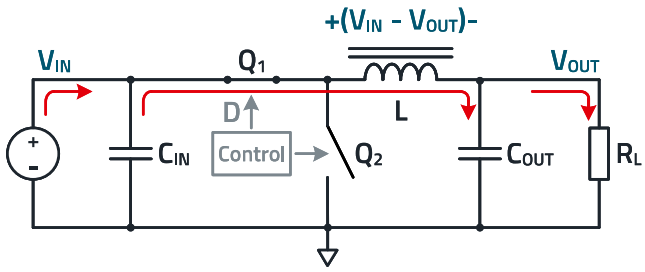


*Figure 5: Buck converter equivalent circuit during $Q_1$ on-time (ideal)*

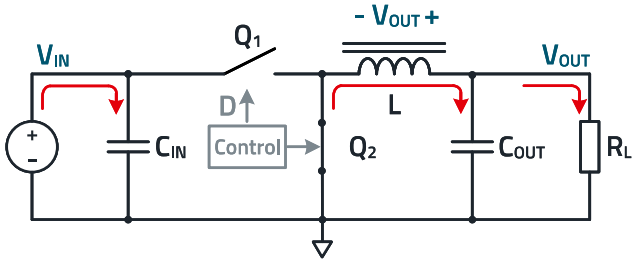


*Figure 6: Buck converter equivalent circuit during $Q_1$ off-time (ideal)*

Therefore, the average inductor current equals the output current:

$$I_L = I_{OUT} \tag{6}$$

An example of deriving (4) by applying volt-second compensation across the inductor is given next. The energy stored in the inductor during the on-time needs to equal energy delivered during the off-time:

$$|\Delta E_{L\_ON}| = |\Delta E_{L\_OFF}| \tag{7}$$

$$\left|\frac{1}{2} \cdot L \cdot \Delta I_{L_{ON}}{}^2\right| = \left|\frac{1}{2} \cdot L \cdot \Delta I_{L_{OFF}}{}^2\right| \tag{8}$$

$$|\Delta I_{L\_ON}| = |\Delta I_{L\_OFF}| \tag{9}$$

Since the inductor time constant (L/R) needs to be higher than the switching period for correct operation, the average voltage across the inductor over a small time window can then be approximated to the 1st order as:

$$V_L = L \cdot \frac{\Delta I_L}{\Delta t} \tag{10}$$

Substituting (10) into (9) for the on or the off-time, the 'volt-second balance' requirement is obtained:

$$|V_{L\_ON} \cdot t_{ON}| = |V_{L\_OFF} \cdot t_{OFF}| \tag{11}$$

Where:

$$t_{ON} = D \cdot T_{SW} \tag{12}$$

$$t_{OFF} = (1 - D) \cdot T_{SW} \tag{13}$$

Previous equations (2) and (4) can also be directly derived from (10) and (11).

Observe how during the off-time, the well-regulated output voltage ($V_{OUT}$) appears across the inductor. This is the base from which additional isolated outputs can be obtained:

$$|V_{L\_OFF}| = V_{OUT} \tag{14}$$

In the buck converter, it is common to approximate:

$$I_{L\_RMS} \approx I_{OUT} \tag{15}$$

However, this will no longer hold valid after adding isolated outputs due to the higher AC-ripple current, as it will be shown in later sections.

## 3. BUCK CONVERTER WITH ISOLATED OUTPUT(S)

### 3.1 Obtaining the Isolated Output(s)

As already introduced, isolated outputs can be obtained from a buck converter by adding coupled windings to the power inductor and a diode-capacitor rectifier circuit to each output (Figure 2). When doing so, one will be using what is commonly called a 'coupled-inductor' or 'energy-storage transformer' (a.k.a. Flyback transformer). Before moving forward, a small clarifying note is provided about the different and often confusing use of these two terms.

### 3.2 Is it Coupled-Inductor or Transformer?

It is not rare to hear the terms 'coupled-inductor' and 'energy-storage transformer' (a.k.a. Flyback transformer) often used interchangeably while referring to the same component in industry. Such passive component is built with a magnetic core featuring an air-gap, allowing it to store energy (this air-gap can be discrete-gap like in solid ferrite cores or distributed like in powdered cores). It also has two or more separate, magnetically coupled windings.

Magnetic component manufacturers like Würth Elektronik normally classify this component in the catalog according to the specific construction techniques employed. If the component is built using standard power inductor assemblies and techniques, like drum cores or iron powder cores for example, then the component is classified as a coupled-inductor (Figure 7). Similarly, if the component is built using common transformer assemblies and techniques (e.g. EP, EE, ER cores, etc) then it is classified as a (flyback) transformer (Figure 8).


*Figure 7: Example Würth Elektronik Coupled Inductors Shielded Drum-core WE-TDC (left), Powdered core WE-MCRI (right)*

*Figure 8: Example Würth Elektronik (energy-storage) Transfomers*

Alternative usages of these terms can also be observed in industry, but this based more on a functional view.

As an example, if the converter could still operate correctly after the magnetic coupling between the windings is removed (e.g. as in a SEPIC), then the component is referred to as a coupled-inductor. Conversely, if after removing the magnetic coupling the converter can no longer operate appropriately, then it is referred to as a 'Flyback' transformer (e.g. as in a Flyback converter).

Differing from this, a different approach is to call it a 'coupled power inductor' in all cases where energy is stored (e.g. as in Flyback and SEPIC converters) and 'transformer' only when there is instantaneous energy transfer without energy storage (e.g. as in Forward and Push-pull converters).

The lack of consensus and different usage of these terms in industry and in catalogs of component manufacturers/vendors can create confusion. In this document, the term 'transformer' will be used in a general sense, without aiming to take sides in the above discussion.

### 3.3. Circuit Analysis

The operation of the buck converter with isolated outputs will be covered in this section focusing on the case of one isolated output (Figure 9), but relevant formulae is also provided for the case of multiple isolated outputs (obtained by correctly scaling the single-output expressions).

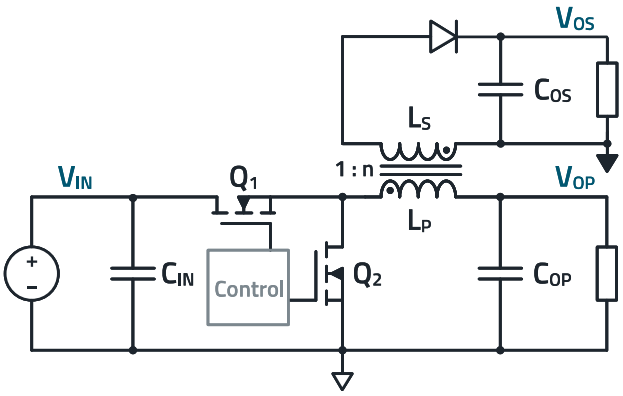


*Figure 9: Synchronous buck converter with isolated output*

The buck converter 'primary' output voltage $V_{OP}$ is set as in (2), and the isolated 'secondary' output voltage $V_{OS}$ can then be set with:

$$V_{OS} = n \cdot V_{OP} \quad (16)$$

where:

$$n = \frac{N_S}{N_P} = \frac{\text{Turns secondary winding}}{\text{Turns primary winding}} \quad (17)$$

Figure 10 and Figure 11 show the equivalent circuit during the on-time and the off-time of $Q_1$, respectively.

During the on-time, the input supply and input capacitor provide energy to the primary output load, to the transformer and to the primary output capacitor ($C_{OP}$), both of which store net energy during this time window (note the difference compared to the standard buck converter, where the output capacitor did not store net energy during the on-time).

Regarding the secondary side circuit, the reflected voltage across the secondary winding is:

$$V_{L_{S\_OFF}} = - n \cdot (V_{IN} - V_{OP}) \quad (18)$$

The rectifier diode is therefore reverse-biased, and no current flows through the secondary winding.

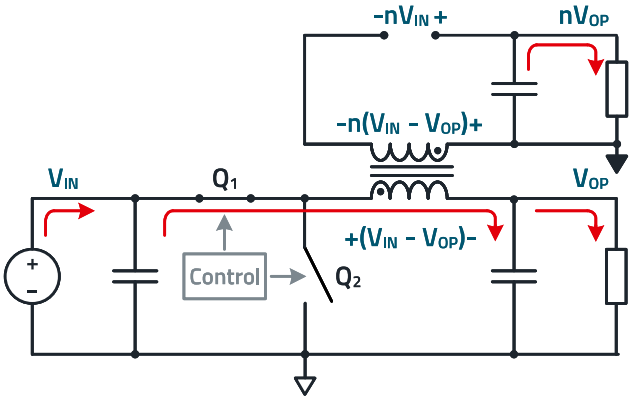


*Figure 10: Circuit during on-time (ideal approximation)*

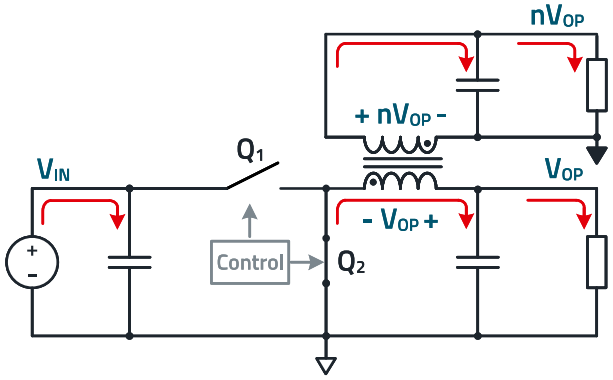


*Figure 11: Circuit during off-time (ideal approximation)*

The diode blocks a voltage given by:

$$V_{D_{OFF}} = - n \cdot V_{IN} \quad (19)$$

The energy required by the isolated output load during the on-time window is provided directly by the secondary output capacitor ($C_{OS}$).

During the off-time window, $Q_1$ is 'open', disconnecting the input supply and input capacitor from the converter output stage and load. This is used by the input supply to recharge the input capacitor. During this time window, energy is transferred to the secondary side, as the transformer delivers now the energy previously stored both to the primary and secondary loads. This is done in so-called 'Flyback-mode', with the energy having been stored during the on-time in the magnetic core air-gap, and being delivered now during the off-time. The primary output capacitor also delivers the energy previously stored, in this case to the secondary output capacitor via the transformer, which transfer the energy in so-called 'Forward-mode'. This means that the energy is transferred 'instantaneously' without any net magnetic field build-up and energy storage in the transformer airgap. The secondary output capacitor stores this energy, which will be used to supply the isolated load during the next on-time window. A detailed analysis and formulae regarding the energy 'flow' in the converter is provided in Appendix A.1 at the end of the document.

Similar to the standard buck converter, the primary output voltage appears across the primary winding during $Q_1$ off-time, and by transformer action, it also appears across the secondary winding scaled by the turns-ratio. The diode then becomes forward-biased, allowing current to flow through the secondary winding and energy transfer from the primary side circuit to the output capacitor and load.

Considering 'ideal' components, and thus ignoring any voltage drops across the diode and component parasitic elements (e.g. resistances, leakage inductance, etc), the secondary winding voltage would then directly appear on the isolated output:

$$V_{L_{S\_OFF}} = n \cdot V_{OP} \approx V_{OS} \quad (20)$$

As we will see in later sections, when considering real components, the result will differ compared to the ideal case shown here.

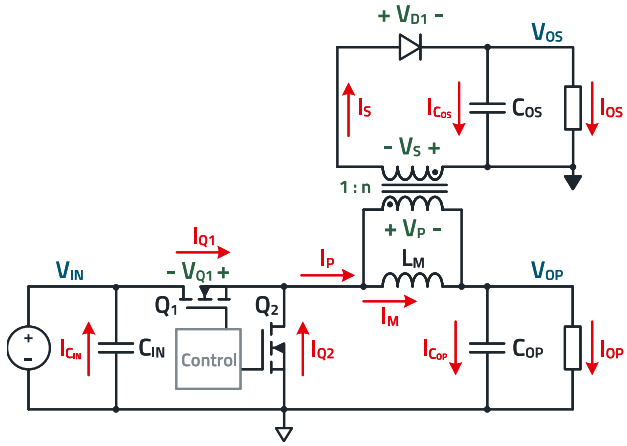


*Figure 12: Reference Waveforms Schematic*

In Figure 13 and Figure 14, the typical switching waveforms of the buck converter with isolated outputs are shown, based on the reference schematic of Figure 12.

Note here how the transformer has been replaced by an inductor in parallel with an ideal transformer. This inductor models the magnetizing inductance ($L_M$) of the transformer, which represents the energy storage function, and it is 'equivalent' to the buck converter inductor. Note that when the isolated load current is zero, the average value of the magnetizing current ($I_M$) equals the primary side output current, as in a standard buck converter.

As the load current on the isolated output(s) increases, the magnetizing current and, in turn, the steady-state energy stored in the magnetic field increase accordingly.

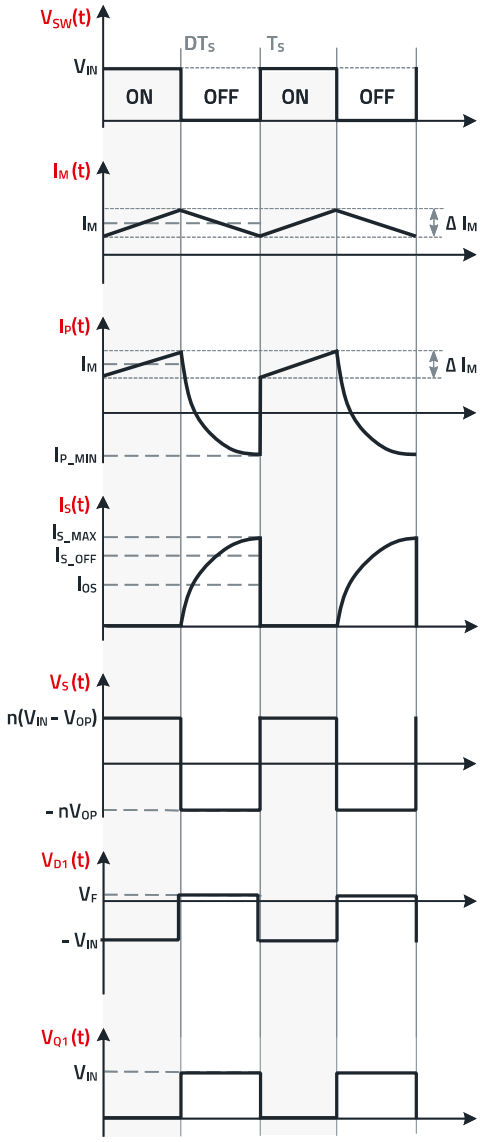


*Figure 13: SW Node and Transformer Waveforms*

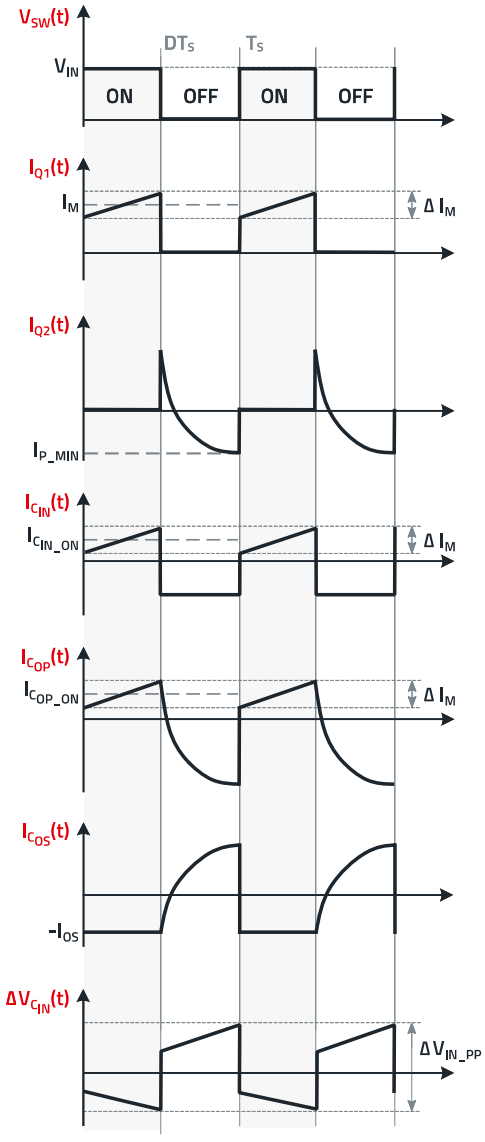


*Figure 14: SW Node, Capacitor and Transistor Waveforms*

The total magnetizing current is a contribution of all output load currents, both on primary and on secondary sides (these scaled accordingly by the corresponding turns-ratio).

For one isolated/secondary output:

$$I_M = I_{OP} + n \cdot I_{OS} \quad (21)$$

For 'k' isolated/secondary outputs:

$$I_M = I_{OP} + \sum_{i=1}^{k} n_i \cdot I_{OS\_i} \quad (22)$$

To correctly estimate the required saturation current rating of the transformer selected, the maximum instantaneous magnetizing current must be considered, since transformer saturation is linked to the maximum magnetic field density that the core can withstand.

Note that the magnetizing current does not necessarily equal the winding current. In this particular case, only during the on-time the primary winding current equals the magnetizing current, and thus the maximum peak value during this time window right at the end of the on-time must be considered.

For one isolated/secondary output:

$$I_{M\_MAX} = I_{OP} + \frac{\Delta I_M}{2} + n \cdot I_{OS} \quad (23)$$

For 'k' isolated/secondary outputs:

$$I_{M\_MAX} = I_{OP} + \frac{\Delta I_M}{2} + \sum_{i=1}^{k} n_i \cdot I_{OS\_i} \quad (24)$$

The term $\Delta I_M$ in the above expressions is the peak-to-peak magnetizing ripple current, and it is obtained as:

$$\Delta I_M = \frac{(V_{IN} - V_{OP}) \cdot D}{L_M \cdot f_{SW}} \quad (25)$$

The magnetizing inductance ($L_M$) is set to limit the magnetizing ripple amplitude. Note that limiting it to 20-40% of the maximum magnetizing current like in a buck converter is not critical when adding isolated outputs, especially when using ferrite-based transformers and MLCC capacitors. A lower $\Delta I_M$ helps to reduce AC core losses (i.e. hysteresis, eddy currents) as well as the peak magnetic field density, providing further margin to saturation. However, when it comes to winding AC losses, which often dominate in this topology, the impact of $\Delta I_M$ will be smaller as winding current amplitude is typically much higher than $\Delta I_M$.

The 'forward-mode' energy transfer during the off-time window (from $C_{OP}$ to $C_{OS}$ via the transformer), with its resulting 'reflected' currents on primary and secondary windings, is what causes the primary winding current amplitude ($\Delta I_P$) to notably differ from the magnetizing current (see Figure 13), with:

$$\Delta I_P = I_{M\_MAX} - I_{P\_MIN} \quad (26)$$

Thus, unlike in a standard synchronous buck converter

$$I_M \neq I_{P_{RMS}} \quad (27)$$

The higher amplitude of the primary winding current would also increase the requirements of $Q_2$, requiring now higher peak and RMS current ratings.

If $C_{OP}$ and $C_{OS}$ are implemented with MLCCs (e.g. WCAP-CSGP series from Würth Elektronik), featuring negligible ESR, the effects on these capacitors caused by a higher RMS current, like temperature rise or voltage ripple, will be negligible in common applications of this topology.

Accurate analytical calculation of the peak-to-peak winding current amplitudes is no trivial task, since these are a higher order function of several parameters, some of which are difficult to measure or estimate accurately, like the leakage inductance. They also depend on the turns-ratio, the duty-cycle, the switching frequency, and the primary and secondary load currents:

$$I_{P\_MIN} = f(n, D, F_{SW}, L_k, I_{OP}, I_{OS}) \quad (28)$$

$$I_{S\_MAX} = f(n, D, F_{SW}, L_k, I_{OS}) \quad (29)$$

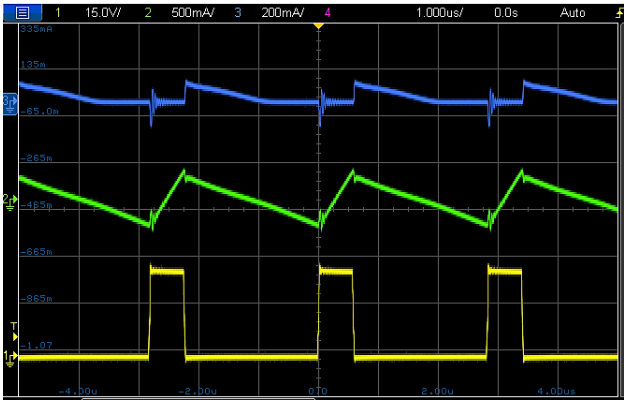


*Figure 15: Experimental Results (light load) ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{IN}$ = 24 V, $V_{OP}$ = 5 V, $I_{OP}$ = 20 mA, $I_{OS}$ = 20 mA, $F_{SW}$ = 350 kHz, L = 22 µH)*

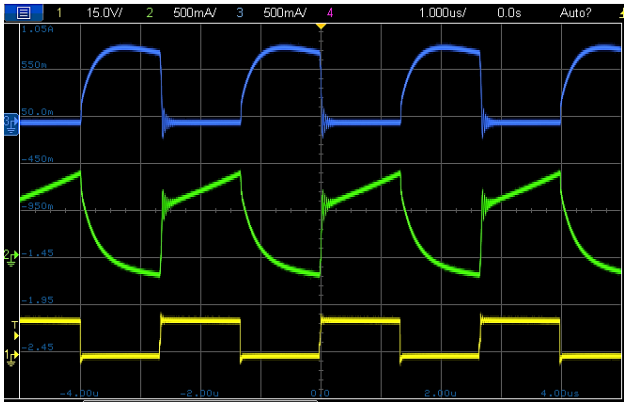


*Figure 16: Experimental Results (full load) ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{IN}$ = 24 V, $V_{OP}$ = 10 V, $I_{OP}$ = 0.3 A, $I_{OS}$ = 0.3 A, $F_{SW}$ = 350 kHz, L = 22 µH)*

The fastest and most accurate approach to finding the above values is by means of a SPICE simulation first, followed by experimental validation on-the-bench once a first prototype is built.

Experimental results obtained with the experimentation board shown in Appendix A.2 are given in Figure 15 and Figure 16, corresponding to light-load and full-load conditions, respectively. It is observed that, when the isolated output current is close to zero (Figure 15), the current measured on the primary winding mostly equals the triangular-shaped magnetizing current, as expected. But a higher order, parabolic current waveshape is observed during the off-time when the isolated output is loaded. This behavior will be explained in more detail in the section 3.4.

For the components not affected by the off-time winding current shape, analytical expressions can be directly obtained.

**Input Capacitor ($C_{IN}$)**

The RMS current through the input capacitor, neglecting effect of $\Delta I_M$ (low-ripple approximation) is calculated as:

$$I_{C_{IN\_RMS}} \approx \left( I_{OP} + \sum_{i=1}^{K} n_i \cdot I_{OS_i} \right) \cdot \sqrt{D \cdot (1 - D)} \qquad (30)$$

The input capacitance is set so that to limit the peak-to-peak input voltage ripple ($\Delta V_{IN\_PP}$) as follows (considering ESR ≃ 0):

$$C_{IN} \approx \frac{\left( I_{OP} + \sum_{i=1}^{K} n_i \cdot I_{OS_i} \right) \cdot D \cdot (1 - D)}{\Delta V_{IN\_PP} \cdot f_{SW}} \qquad (31)$$

Normally, a maximum ripple amplitude below 0.5% of the minimum input voltage is recommended.

**Control Transistor ($Q_1$)**

The RMS current through the control MOSFET is:

$$I_{Q1\_RMS} \approx \left( I_{OP} + \sum_{i=1}^{K} n_i \cdot I_{OS_i} \right) \cdot \sqrt{D} \qquad (32)$$

The maximum peak current is calculated as:

$$I_{Q1\_PK} = I_{OP} + \sum_{i=1}^{K} n_i \cdot I_{OS_i} + \frac{\Delta I_M}{2} \qquad (33)$$

**Rectifier Diode ($D_1$)**

The average current though the rectifier diode is the secondary winding current, which in turn, equals the secondary load current:

$$I_{D_1\_AV} = I_S = I_{OS} \qquad (34)$$

During the on-time, the secondary-side rectifier diode will block a voltage given by:

$$V_{D_1\_ON} = n \cdot V_{IN\_MAX} \qquad (35)$$

In order to obtain approximate analytical expressions of RMS current in transformer windings and low-side MOSFET ($Q_2$), a 1st-order approximation of the parabolic primary and secondary current waveforms is proposed in the section 3.4.

### 3.3 The Isolated Output(s) Current Waveform

During the switching transition between conduction and blocking states of the control transistor $Q_1$, the voltage across the transformer windings quickly changes polarity, appearing as a voltage step across the primary and secondary windings.

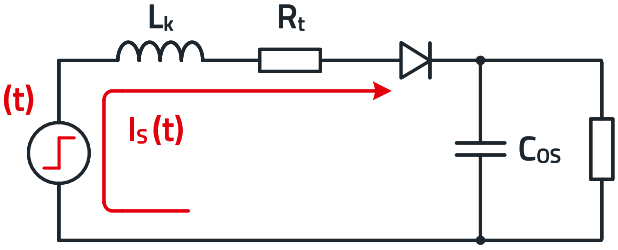


*Figure 17: Secondary side RLC network*

A closer look at the secondary side circuit will reveal an equivalent RLC network with a series diode. This is formed by the transformer leakage inductance referred to the secondary side $L_k$, output capacitance $C_{OS}$, parasitic

resistance referred to secondary side ($R_t$) as well as load resistance ($R_L$), as shown in Figure 17. Note that from a time-domain perspective, such 2nd order network has two time constants, one associated with the leakage inductance, and the other with the output capacitance.

After the voltage step is applied, the diode becomes forward-biased and energy can be transferred from primary to secondary side. However, the secondary current $I_S(t)$ cannot increase instantaneously due to the presence of the leakage inductance. For a fixed output capacitance ($C_{OS}$), the secondary current waveshape observed during the off-time will mainly depend on how the time constant formed by the leakage inductance and the total resistance ($\tau_{Lk} = L_k / R_t$) compares to the duration of the off-time window during which energy is transferred to the secondary side ($t_{OFF} = (1 - D) \cdot T_{SW}$).

Note that the total resistance includes not only the winding resistance, but also the $R_{DS(ON)}$ of the low-side MOSFET on the primary side and the ESR of the output capacitor.

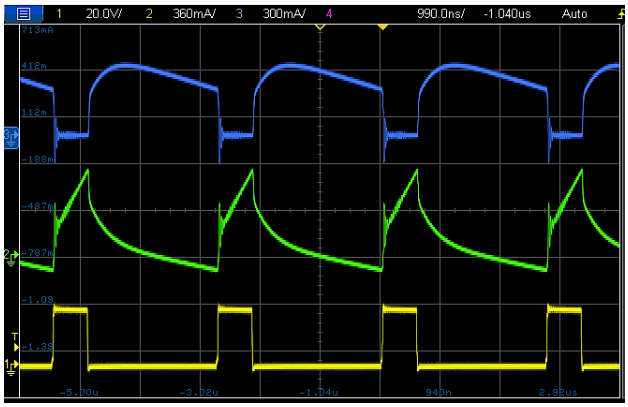


*Figure 18: Experimental Results for $t_{OFF}$ = 2.2 µs ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{OP}$ = 5 V, D = 20%, $I_{OP}$ = 0.1 A, $I_{OS}$ = 0.3 A, $F_{SW}$ = 350 kHz, L = 22 µH)*

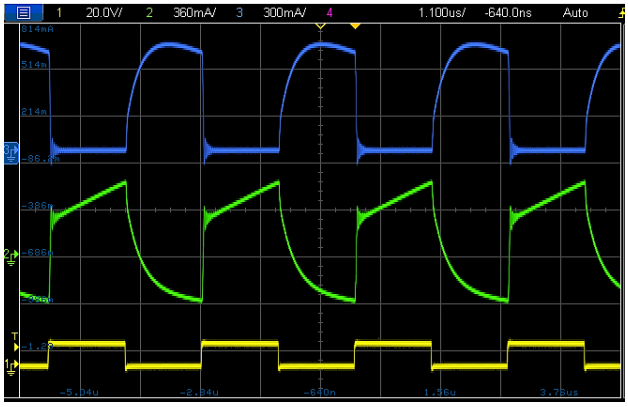


*Figure 19: Experimental Results for $t_{OFF}$ = 1.42 µs ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{OP}$ = 5 V, D = 50%, $I_{OP}$ = 0.1 A, $I_{OS}$ = 0.3 A, $F_{SW}$ = 350 kHz, L = 22 µH)*

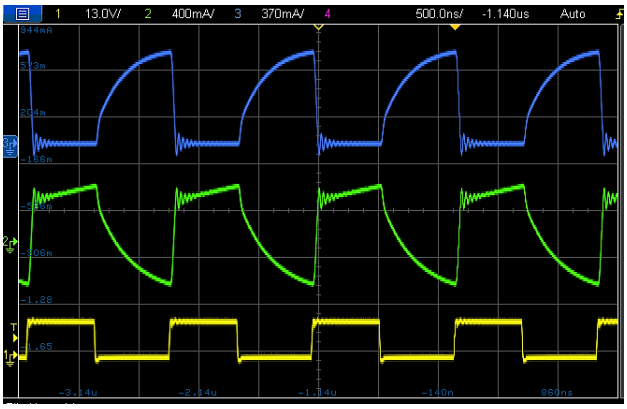


*Figure 20: Experimental Results for $t_{OFF}$ = 0.58 µs ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{OP}$ = 5 V, D = 50%, $I_{OP}$ = 0.1 A, $I_{OS}$ = 0.3 A, $F_{SW}$ = 850 kHz, L = 22 µH)*

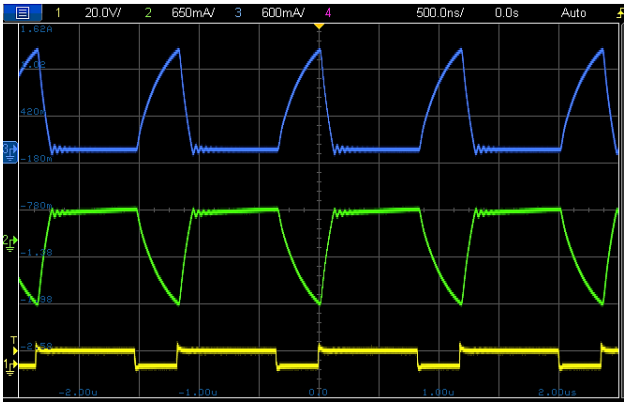


*Figure 21: Experimental Results for $t_{OFF}$ = 0.35 µs ($V_{SW}$ (), $I_P$ (), $I_S$ ()) ($V_{OP}$ = 5 V, D = 70%, $I_{OP}$ = 0.1 A, $I_{OS}$ = 0.3 A, $F_{SW}$ = 850 kHz, L = 22 µH)*

For $\tau_{Lk} << t_{OFF}$, the current waveform will be parabolic (Figure 18 and Figure 19), whereas for $\tau_{Lk} \geq t_{OFF}$, the waveform will approach a 1st-order-like rising slope or triangular shape, as the energy transfer window will end before the time constant is reached (Figure 20 and Figure 21).

For the results shown in Figure 18 to Figure 21, the design uses Würth Elektronik DPC-HV 7448841220 (with winding resistances $R_P = R_S$ = 455 mΩ and leakage inductance $L_k$ = 0.41 µH). The controller is the LM5160 (Texas Instruments) with $Q_2$ - $R_{DS(ON)}$ = 130 mΩ. This yields $R_t \simeq 1\ \Omega$ neglecting the ESR of the output MLCC capacitors (WCAP-CSGP series). The time constant is $\tau_{Lk} \approx 0.41$ µs. In the figures, the off-time window is varied by changing the duty-cycle and switching frequency as highlighted in red.

It is observed that the secondary current waveshape determines the peak and RMS values of the current through the transformer windings and $Q_2$ transistor.

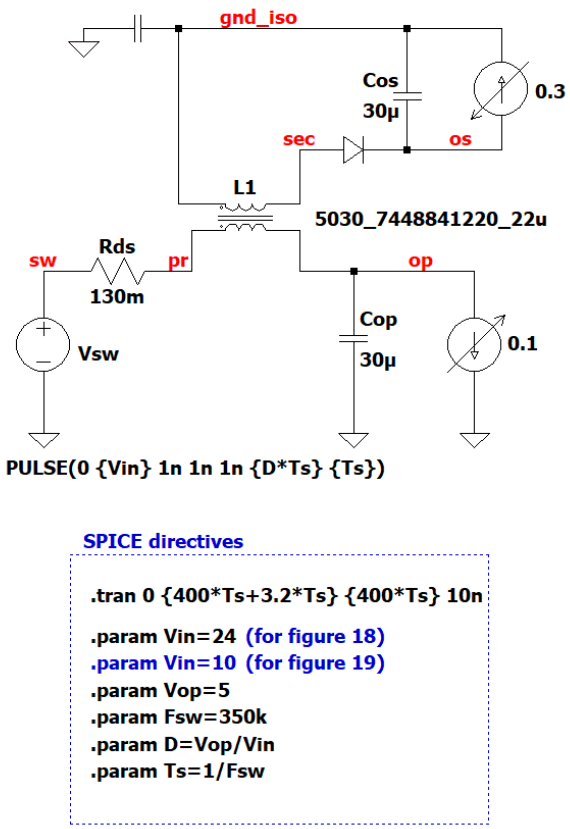


*Figure 22 : LTspice simple simulation fixture*

Obtaining an accurate estimation of these values early in the design stage is necessary in order to select the controller IC and/or external transistor devices as well as the transformer.

A good estimation can be obtained by means of a SPICE simulation using Würth Elektronik SPICE models. The simple simulation fixture of the power stage in open-loop configuration shown in Figure 22 can be used for this purpose (here with the SPICE model of the coupled-inductor DPC-HV 7448841220, and 10 mΩ ESR of output capacitors).

The circuit is simulated in LTspice with the specifications of Figure 18 and of those of Figure 19.

The results are shown in Figure 23 and Figure 24, respectively, confirming a good agreement between the simulated and experimental waveforms and amplitude values.

Note how in the circuit of Figure 22, the switch-node waveform ($V_{SW}$) is directly fed to the output stage for simplification, instead of using the traditional switching network ($Q_1$ and $Q_2$). Despite this, the peak current requirements for the high-side and low-side transistors can be directly obtained from the primary winding current waveform (see also section 4.3).

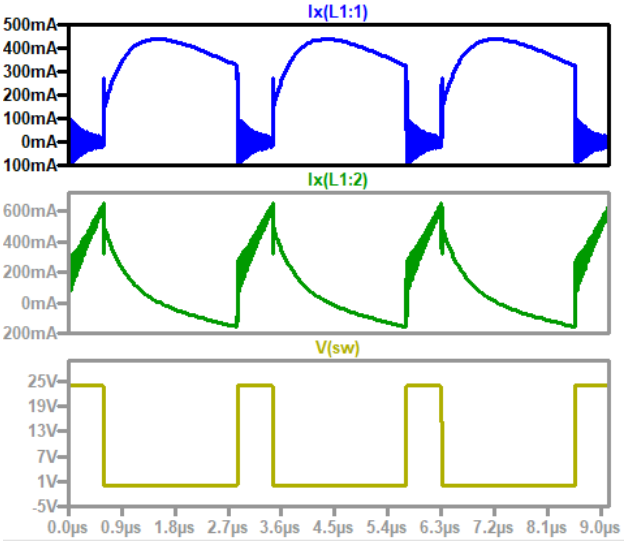


*Figure 23: LTspice simulation results for specification of Figure 18*

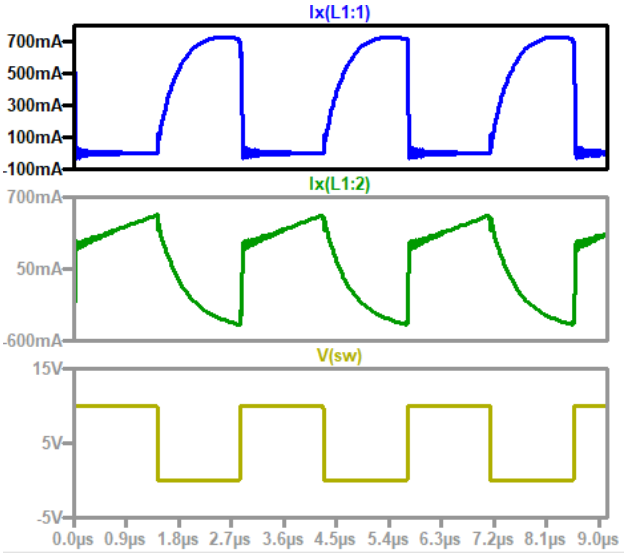


*Figure 24: LTspice simulation results for specification of Figure 19*

In addition, the RMS current for $Q_2$ can be obtained by substracting the result in previous (32) ($Q_{1,RMS}$) from the primary winding current RMS value measured in simulation.

Alternatively, the full circuit with the switching network can also be easily implemented.

### 3.4 The Isolated Output(s) Voltage Regulation

In a converter with 'ideal' components and thus no parasitic elements, the output voltage on the secondary output(s) would accurately track the regulated primary output voltage, scaled by the corresponding transformer turns-ratio, under all load current and operating conditions. However, the parasitic elements of 'real-world' components have an

impact on the resulting voltage level obtained on the isolated output(s).

Figure 25 shows the equivalent circuit during the off-time window with the main parasitic elements, and considering a transformer with only one isolated output and a 1:1 winding turns-ratio.

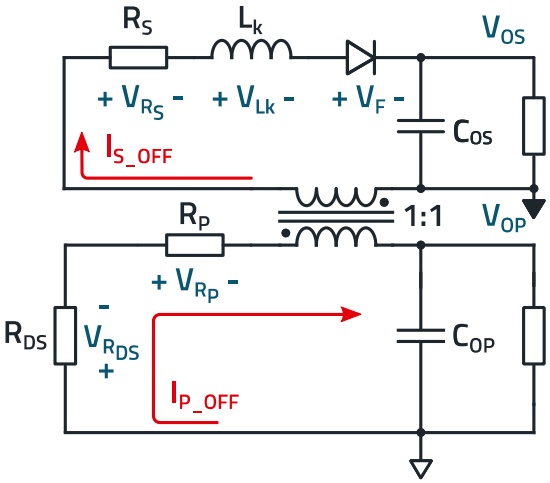


*Figure 25: Equivalent circuit during off-time with parasitic elements*

The parasitic elements represented are the on-resistance of the low-side MOSFET ($R_{DS}$), the primary winding resistance ($R_P$), the secondary winding resistance ($R_S$) and the transformer leakage inductance referred to the secondary side ($L_k$). In addition, the non-linear forward voltage drop across the diode must also be considered, as it dominates regulation especially at low output currents and voltages.

The average voltage drops during the off-time window across each of these parasitic elements will determine the resulting voltage on the isolated output, as follows:

$$V_{OS} = V_{OP} + V_{R_{DS}} + V_{R_P} - V_f - V_{L_k} - V_{R_S} \quad (36)$$

where:

$$V_{R_{DS}} = I_{P\_OFF} \cdot R_{DS} \quad (37)$$

$$V_{R_P} = I_{P\_OFF} \cdot R_P \quad (38)$$

$$V_{R_S} = I_{S\_OFF} \cdot R_S \quad (39)$$

In the previous formulae, $I_{P\_OFF}$ and $I_{S\_OFF}$ are the average primary and secondary winding currents during the off-time, respectively, as shown in Figure 26.

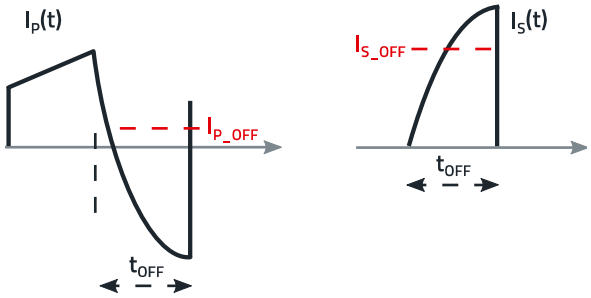


*Figure 26: Primary and secondary currents showing average values during off-time (red)*

The value of $I_{P\_OFF}$ depends on the primary output current ($I_{OP}$), the duty-cycle (D) as well as the corresponding turns-ratio (n) and load current ($I_{OS}$) on each isolated output.

For one isolated output:

$$I_{P\_OFF} = I_{OP} - \frac{D}{(1 - D)} \cdot n \cdot I_{OS} \quad (40)$$

For 'k' isolated outputs:

$$I_{P\_OFF} = I_{OP} - \frac{D}{(1 - D)} \cdot \sum_{i=1}^{k} n_i \cdot I_{os_i} \quad (41)$$

Regarding the secondary winding(s) current, it is a function of the respective isolated output current and the duty-cycle:

$$I_{S\_OFF} = \frac{I_{OS}}{(1 - D)} \quad (42)$$

Going back to the voltage drop analysis, the average voltage drop across the diode during the off-time can be obtained from the I-V curve found in its datasheet:

$$V_f = V_D \ (@ \ I_{S\_OFF}) \quad (43)$$

The voltage drop across the leakage inductance during the off-time is more complex to estimate accurately. Its instantaneous value is given as:

$$V_{L_k}(t) = L_k \cdot \frac{di_{S\_OFF}(t)}{dt} \quad (44)$$

The average voltage drop during the off-time can then be obtained as follows:

$$V_{L_k\_OFF} = L_k \cdot \frac{\Delta I_{OFF}}{t_{OFF}} \quad (45)$$

It is observed that $V_{Lk\_OFF}$ depends on the delta of the secondary winding current between start and end of the off-time window ($\Delta I_{OFF}$). Note that $\Delta I_{OFF}$ only refers to

the AC winding reflected currents (e.g. from the forward mode energy transfer).

For a triangular-shaped secondary current waveform (i.e. like in Figure 22) the following approximation can be performed, observing previous (42):

$$V_{Lk\_OFF} \approx L_k \cdot \frac{2 \cdot I_{OS} \cdot F_{SW}}{(1 - D)^2} \qquad (46)$$

This shows that the net voltage drop across the leakage inductance during the off-time increases with the isolated load current, the duty cycle, and the leakage inductance value itself.

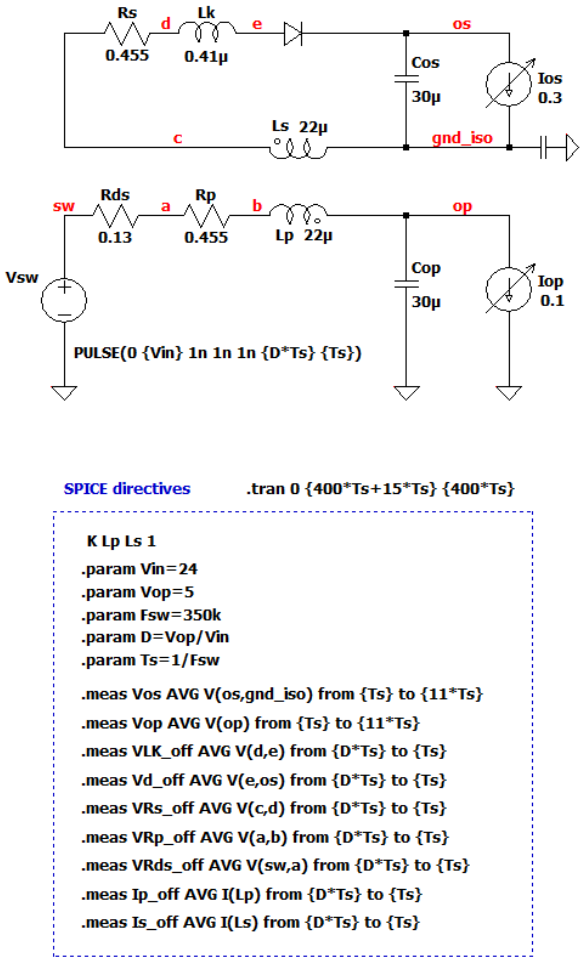


*Figure 27: LTspice simulation setup for element-wise voltage drop analysis during off-time*

```
vos: AVG(v(os,gnd_iso))=3.92114 FROM 2.85714e-006 TO 3.14286e-005
vop: AVG(v(op))=4.94986 FROM 2.85714e-006 TO 3.14286e-005
vlk_off: AVG(v(d,e))=0.0640176 FROM 5.95238e-007 TO 2.85714e-006
vd_off: AVG(v(e,os))=0.780861 FROM 5.95238e-007 TO 2.85714e-006
vrs_off: AVG(v(c,d))=0.170944 FROM 5.95238e-007 TO 2.85714e-006
vrp_off: AVG(v(a,b))=0.0109152 FROM 5.95238e-007 TO 2.85714e-006
vrds_off: AVG(v(sw,a))=0.00311864 FROM 5.95238e-007 TO 2.85714e-006
ip_off: AVG(i(lp))=0.0239895 FROM 5.95238e-007 TO 2.85714e-006
is_off: AVG(i(ls))=0.375701 FROM 5.95238e-007 TO 2.85714e-006
```

*Figure 28: Measured values from 'SPICE Error Log' file*

An LTspice simulation fixture based on the specification of Figure 19 is shown in Figure 27, which can be used in order to confirm the validity of the previous analysis. In addition, it is observed how $V_{Lk\_OFF}$ is the only voltage drop impacted by the switching frequency.

A word of caution: the (46) formula has only been derived in order to provide insight of the parameter dependence of $V_{Lk\_OFF}$, and it would only be accurate for purely triangular current waveform, but not for the parabolic case (which is most common).

Note that the voltage drops during the off-time are obtained with the '.MEASURE' command in SPICE. Note also that the ESR of both output capacitors is set to 10 mΩ (not shown in the schematic). The simulated values are retrieved from the 'SPICE Error Log' file (see Figure 28):

Based on previous analysis, the calculated values are as follows:

From (42), for D = 0.2 and $T_{SW}$ = 3.33 µs, it is obtained:

$$I_{OS} = 0.376 \text{ A}$$

From (40), it is obtained:

$$I_{P\_OFF} = 0.024 \text{ A}$$

From (37), (38) and (39), it is obtained:

$$V_{R_{DS}} = 3.12 \text{ mV}$$

$$V_{R_P} = 10.9 \text{ mV}$$

$$V_{R_S} = 171 \text{ mV}$$

These values correspond with those obtained in simulation. The voltage drop across the leakage inductance during the off-time is in this case only 64 mV, due to optimal operating conditions with a low duty-cycle and low value of leakage inductance of the DPC-HV coupled-inductor. In this example case, the diode forward voltage drop ($V_{D\_OFF}$ = 0.781 V) is the main contributor degrading regulation.

Adding up these voltage drops based on previous (36), it is obtained: $V_{OS}$ = 3.92 V, in agreement with the simulation result.

As observed in this case, selecting a diode with a very low forward voltage drop (e.g. Schottky type) would considerably improve output voltage regulation. However, as the duty-

cycle or switching frequency increases, the voltage drop across the leakage inductance starts to gain importance. For the same specification of Figure 27, but with a higher duty-cycle of 50% ($V_{OP}$ = 12 V) and switching frequency of 600 kHz, the voltage drop across the leakage inductance increases now to 0.41 V, becoming the second most dominant after the diode.

In the simulation shown in Figure 27, the DPC-HV 7448841220 coupled-inductor had been replaced by its parasitic elements in order to measure individual voltage drops. Running the same simulation with the SPICE model of the 7448841220 coupled-inductor as in Figure 22, the isolated output voltage obtained is $V_{OS}$ = 3.91 V, which is also in very good agreement with previous results.

Experimental results for this specification, showing the output voltage levels on primary and secondary outputs are shown in Figure 29. The isolated output voltage observed is $V_{OS}$ = 4.21 V. The discrepancy here compared to simulation results ($V_{OS}$ = 3.93 V) lies in the diode forward voltage drop. In the simulation, a standard diode model was used with $V_F$ = 0.785 V, whereas the diode used in the prototype shows an average voltage drop during the off time of around 0.25 to 0.3 V (see Figure 30). Correcting for this, the output voltage obtained in simulation if the correct diode SPICE model had been used would be in the range of 4.18 to 4.23 V, matching very well the experimental results.

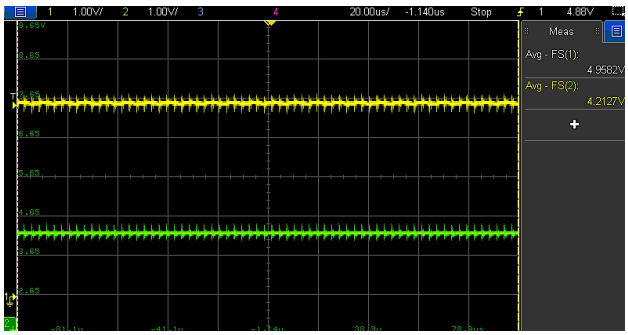

*Figure 29: Experimental results ($V_{OP}$ (), $V_{OS}$ ())*

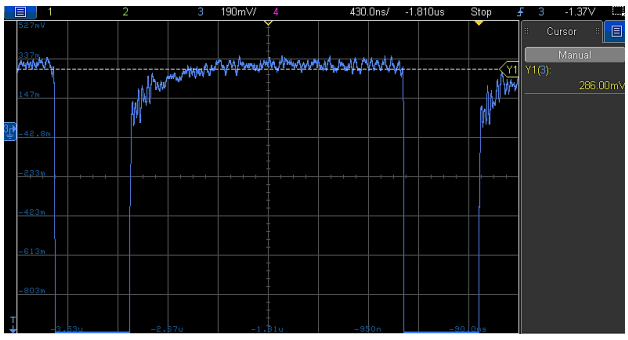

*Figure 30: Experimental result for Diode average forward voltage drop during off-time*

This shows the importance of using accurate SPICE models, specially for the secondary diode and the transformer in this topology. When doing so, SPICE simulation can yield very accurate results. Note that Würth Elektronik SPICE models are currently available by default in LTspice library. In addition, SPICE models for PSPICE simulator are also available and can be downloaded from Würth Elektronik website.

### 3.5 Experimental Results: $V_{OS}$ Regulation

The following experimental results examples show the variation of the isolated output voltage as the isolated load current ($I_{OS}$), the switching frequency ($F_{SW}$), the duty cycle (D), the leakage inductance ($L_k$) and/or the winding resistances ($R_P$ and $R_S$) increase (see Appendix A.3 for details of the evaluation board used for these measurements).

In Figure 31, the impact on the isolated output voltage level of the increasing voltage drop across the leakage inductance due to a higher switching frequency (i.e. shorter off-time) can be observed.

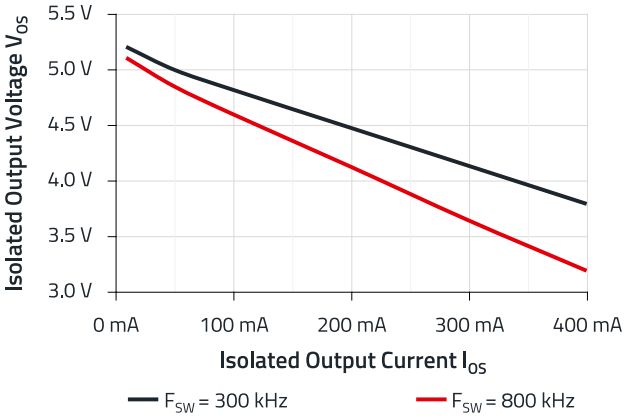


*Figure 31: $V_{OS}$ vs $I_{OS}$ @ $F_{SW}$*
*($V_{IN}$ = 10 V, $V_{OP}$ = 5 V, $I_{OP}$ = 0.4 A, D = 0.5, L = DPC-HV 22 µH)*

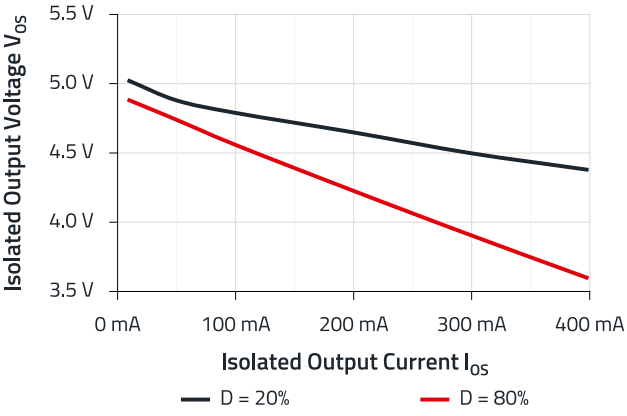


*Figure 32: $V_{OS}$ vs $I_{OS}$ @ Duty-cycle (D)*
*($V_{OP}$ = 5 V, $I_{OP}$ = 0.4 A, $F_{SW}$ = 300 kHz, L = TDC-HV 22 µH)*

In Figure 32, it can be clearly seen how, for a set switching frequency, a higher duty-cycle negatively affects the isolated output voltage level, due again to a shorter off-time window.

The off-time corresponds to the energy transfer window from primary to secondary sides, and as this becomes shorter, a higher secondary current peak is required to transfer the same amount of energy. This, in turn, increases the voltage drops across elements like resistances and leakage inductance, resulting in a lower isolated output voltage level.

In Figure 33, for a fixed operating condition, the impact of higher values of parasitic winding resistances and leakage inductance is observed. As these parasitic elements increase, so do the voltage drops across them for the same off-time window, causing a higher reduction of the isolated output voltage.

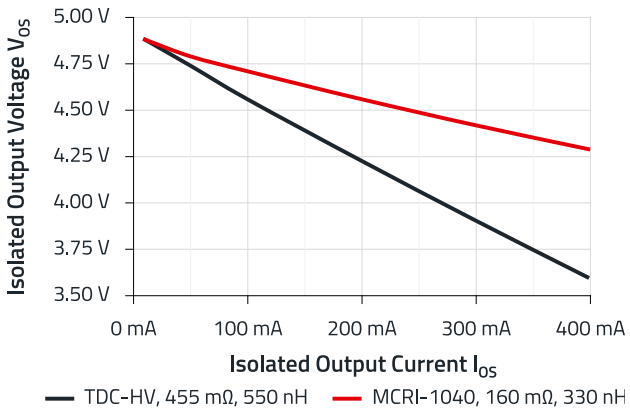


*Figure 33: $V_{OS}$ vs $I_{OS}$ @ ($R_P$, $R_S$ and $L_k$)*
*($V_{IN}$ = 10 V, $V_{OP}$ = 5 V, $I_{OP}$ = 0.4 A, D = 0.5, $F_{SW}$ = 300 kHz, L = 22 µH)*

**Cross-regulation (primary-secondary)**

The voltage drops across the parasitic elements $R_{DS(ON)}$ and $R_P$ on the primary side circuit during the off-time window (which are directly proportional to $I_{P\_OFF}$), will cause the resulting voltage across the primary winding, and in turn, the reflected voltage to the secondary winding, to be lower or higher than the regulated output voltage $V_{OP}$, depending on whether $I_{P\_OFF}$ is positive or negative, respectively (refer to Figure 26).

This effect can be observed in the experimental results shown in Figure 34. Here, keeping the isolated load current fixed at light load, it is seen how an increase in the primary load current and thus in $I_{P\_OFF}$, causes the isolated output voltage to rise, as expected from previous (36):

$$V_{OS} = V_{OP} + V_{R_{DS}} + V_{R_P} - V_f - V_{L_k} - V_{R_S} \qquad (47)$$

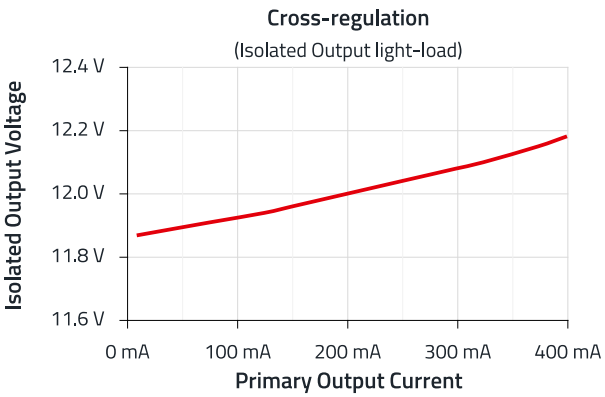


*Figure 34: $V_{OS}$ vs $I_{OP}$*
*($V_{IN}$ = 24 V, $V_{OP}$ = 12 V, $I_{OS}$ = 10 mA, $F_{SW}$ = 350 kHz, L = 22 µH)*

This shows how a higher primary output load current can actually help to 'offset' the negative voltage drops on the secondary side.

In the case of several isolated outputs, the load current on each of these isolated rails will impact the value of $I_{P\_OFF}$, as they are reflected to the primary-side circuit scaled by the turns-ratio. This, in turn, will affect the voltage regulation on the other isolated output rails, leading to a cross-regulation effect. Again, SPICE simulation and experimental results can help to accurately measure the extent of this effect in a particular specification in order to meet the target voltage regulation.

## 4. IMPORTANT DESIGN CONSIDERATIONS

### 4.1 Improving Isolated Output Voltage Regulation

There are several design considerations which can help to improve the voltage regulation of the isolated output rail(s), as summarized here.

**Selection of components and operating conditions**

Based on the analysis and results of previous sections, regulation of the isolated output voltage could be improve with:

- Lower transformer leakage inductance
- Lower transformer DCR
- Lower duty cycle
- Lower switching frequency
- Lower $V_f$ diode (e.g. Schottky type) on secondary side(s)

Note that a trade-off needs to be found amongst the above parameters in order to additionally keep a small solution size and good efficiency, making this topology still competitive against alternative options.

**Additional Output Regulation Stage**

For applications requiring tightly regulated output voltage rails with very low voltage ripple, like for example, signal conditioning circuits with high-precision amplifiers or Analog-to-Digital Converters (ADC), an additional regulation stage can be added to the converter outputs as depicted in Figure 35.

One of the options to implement this regulation stage is with low-dropout linear voltage regulators (a.k.a LDOs), with actual devices providing excellent voltage accuracy down to 0.5% as well as high voltage ripple attenuation (PSRR). One important design consideration when using LDOs is to ensure that the isolated output voltage at full-load current ($V_{OS\_MIN}$) is still higher than the desired regulated output voltage ($V_{OS\_reg}$) plus the minimum allowable dropout voltage across the LDO-IC device ($V_{LDO\_MIN}$), as given in its datasheet:

$$V_{OS\_MIN} > V_{OS\_REG} + V_{LDO\_MIN} \quad (48)$$

The main drawback of LDOs is that they are highly inefficient since they are in fact a 'pass-transistor' which can be effectively modelled as a variable resistor. As the step-down ratio and load current increase, the power dissipation becomes excessive, severely affecting efficiency and requiring bigger copper heatsink area for adequate thermal management, resulting in a bigger solution size. For this reason, LDOs are limited to very low load current applications.

For higher current applications where small size is paramount, a DC-DC step-down Micromodule IC can be used (e.g. Magi³C-VDMM series from Würth Elektronik). Since Micromodules are in fact switching regulators, they can supply higher output currents with very high efficiency and thus low temperature rise, helping to keep a small solution size.

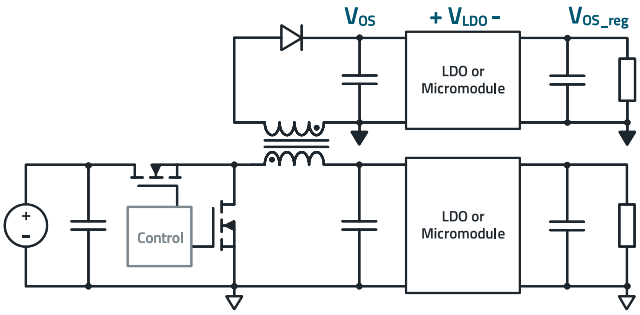


*Figure 35: Example additional regulation stage*

**Using a Buck-boost converter topology**

A buck-boost topology with isolated output(s) (Figure 36) can be used in applications where the primary output rail is not used, or alternatively in those requiring outputs with inverted polarity with respect to the input rail, as in the case of non-isolated bipolar supply voltages.

In the buck-boost topology, the voltage across the inductor during the off-time also equals the regulated output voltage, which allows for creating additional isolated outputs in the same way as for the buck topology. However, a buck-boost power stage can provide tighter regulation of the isolated output voltage compared to a buck topology, especially as the voltage conversion ratio increases.

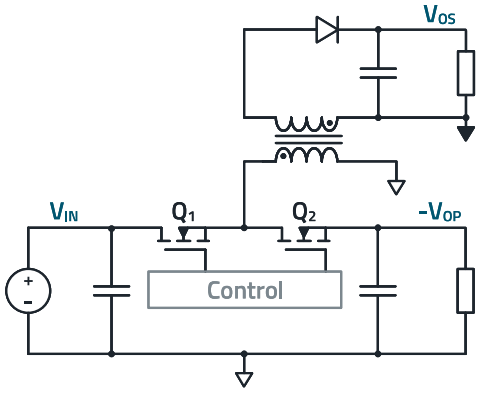


*Figure 36: Example synchronous Buck-boost with Isolated Output*

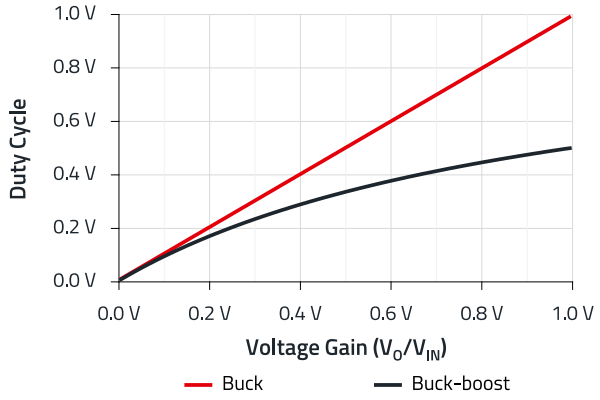


*Figure 37: Voltage Conversion Ratio vs Duty Cycle Comparison*

The reason for this is that, for a set conversion ratio, the buck-boost converter will operate at a lower duty-cycle than a buck power stage ((49) and (50)), as shown in Figure 37. The lower the duty cycle, the longer the off-time window and in turn, the lower the average parasitic voltage drops during the off-time. From Figure 37, a performance improvement is expected especially for duty-cycles exceeding 50%.

$$\text{Buck} \rightarrow \left|\frac{V_{OUT}}{V_{IN}}\right| = D \qquad (49)$$

$$\text{Buck-boost} \rightarrow \left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{D}{1 - D} \qquad (50)$$

An example of how the output voltage regulation can considerably improve with a buck-boost topology is shown in the SPICE simulation results of Figure 38.

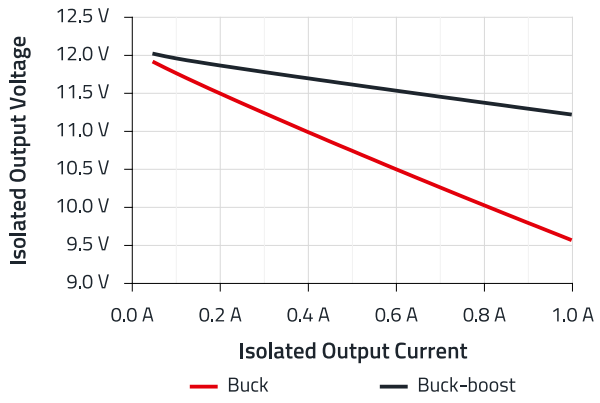


*Figure 38: $V_{OS}$ Regulation - Buck vs Buck-boost Example Comparison ($V_{IN}$ = 18 V, $V_{OP}$ = 12.7 V, $I_{OP}$ = 0.1 A, $F_{SW}$ = 350 kHz, $L_M$ = 47 µH, $L_k$ = 200 nH, n = 1)*

### 4.2 Why using a Synchronous Converter?

In low-power synchronous converters, both 'electronic switches' $Q_1$ and $Q_2$ are implemented using transistors (typ. MOSFETs), and they are usually directly controlled by the IC controller logic and driver. In a non-synchronous converter (Figure 39), only the control switch is a transistor, and a diode is then used for the complementary switch.

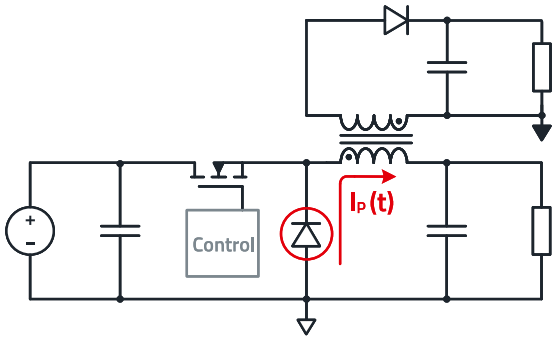


*Figure 39: Non-synchronous Isolated-Output Buck Converter*

Unlike a MOSFET, which can conduct current bidirectionally across drain and source terminals, the power diode can only conduct current in one direction, from anode to cathode, thus not allowing the inductor winding current of the buck converter to reverse direction.

During the off-time in the buck converter with isolated output topology, energy is transferred to the secondary side and, depending on the value of several component parameters and operating conditions, the instantaneous primary winding current may become negative during part of the off-time. In a non-synchronous buck converter this cannot happen because of the single-quadrant conduction of the diode, and as a consequence, the amount of energy delivered to the secondary side will be limited (Figure 40). This will cause the secondary output voltage to droop or collapse, an issue which is avoided when using a synchronous buck power stage.

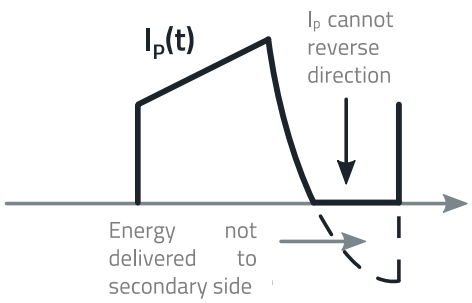


*Figure 40: Energy transfer limitation of non-synchronous converter*

Figure 41, Figure 42 and Figure 43 show SPICE simulation results for a non-synchronous buck converter in a typical application specification. The converter supplies the isolated load with 100 mA at around 5 V. After the primary output load current demand reduces from 500 mA to 50 mA (light-load), the isolated output voltage collapses to 1.2 V since the required energy cannot be supplied during the off-time as the current cannot reverse direction.

Note that a similar behavior would happen if the isolated load current is stepped up from light load to full-load while the primary output current is low. But despite this limitation, non-synchronous buck converters can in practice still be used, albeit with a very careful design. It is necessary to ensure that the primary output be constantly loaded, with the level of primary load current needed at every moment directly depending on the secondary load current demand, which negatively impacts efficiency and thermal performance.

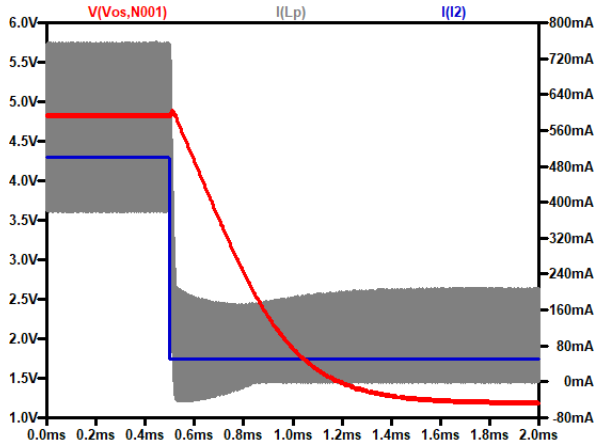


*Figure 41: LTspice simulation: Isolated output voltage after primary output current load step from 500 mA to 50 mA in a non-synchronous buck converter with isolated output ($V_{OS}$ (I), $I_{OP}$ (I), $I_P$ (I)) ($V_{IN}$ = 24 V, $V_{OP}$ = 5 V, $I_{OS}$ = 0.1 A, $I_{OP}$ = 0.5 A to 0.05 A, $F_{SW}$ = 300 kHz)*

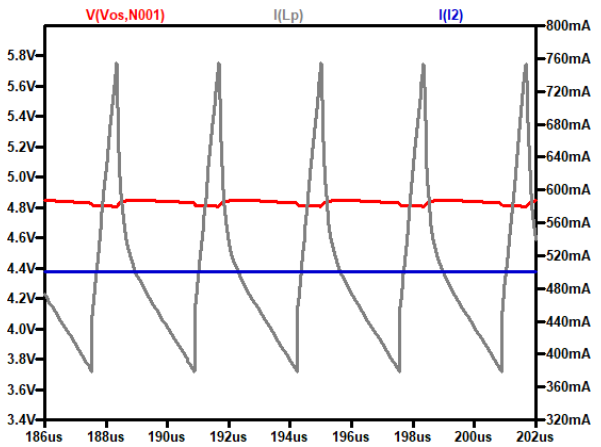


*Figure 42: Zoomed in at around 0.2 ms ($V_{OS}$ (I), $I_{OP}$ (I), $I_P$ (I))*

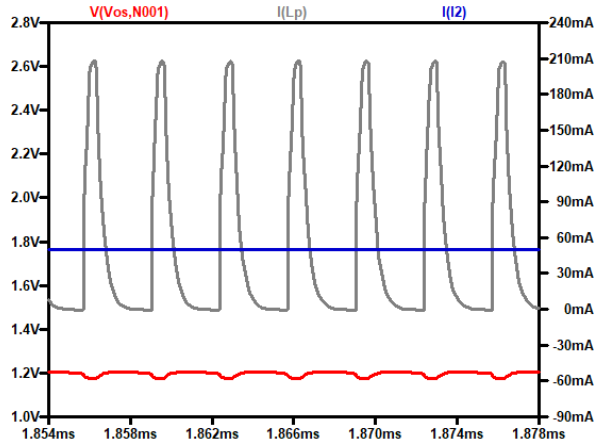


*Figure 43: Zoomed in at around 1.87 ms ($V_{OS}$ (I), $I_{OP}$ (I), $I_P$ (I))*

A synchronous buck converter is the recommended solution both for better performance and a for a more reliable design. There is also a wide availability of cost-effective, monolithic synchronous IC buck controllers with simple, easy-to-design control loop, like the LM5160 or the LM5017 with Constant ON-time (COT) from Texas Instruments Inc, for example.

### 4.3. Output Power Limitation

The practical output power limit for the isolated-output buck converter, as with any other topology, is the value above which alternative topologies would present more advantages based on the specifications of target applications (e.g. regarding size, cost, performance, etc).

Based on this, the buck converter with isolated outputs is currently used in applications with power levels up to around 15 W (all outputs combined). In most applications, however, the output power is found below 5 W. In this lower power range this topology can successfully compete against popular alternatives like the primary-side-regulated (PSR) flyback or push-pull topologies, in particular regarding efficiency, small size, low cost and design simplicity.

To achieve a simple and compact solution, DC-DC converter ICs with integrated MOSFET transistors are widely used. But this also has the drawback that the maximum output power of the converter will be limited by the characteristics of the internal transistors and IC package.

As the primary and secondary load current of the converter, and in turn the overall output power increases, the primary winding current amplitude will also increase, eventually reaching the current limits of the internal MOSFETs (Figure 44).

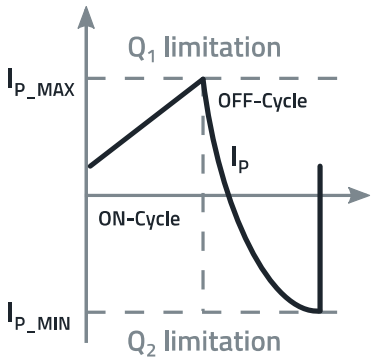


*Figure 44: Primary winding current and transistor peak-current limits*

Since the current through $Q_1$ equals the primary winding current during the on-time, $Q_1$ peak current rating directly limits the total combined maximum converter output current, as shown below for a one-isolated-output solution:

$$I_{Q1(MAX\_PK)} > I_{M\_MAX} = I_{OP} + n \cdot I_{OS} + \frac{\Delta I_M}{2} \quad (51)$$

Current through $Q_2$ equals the primary winding current during the off-time. For a set operating condition, $Q_2$ peak current sink rating will limit the total current on the isolated outputs. Accurate value of the minimum peak current can be obtained via SPICE simulation, as shown before.

$$I_{Q2(MAX\_SINK\_PK)} > |I_{P\_MIN}|$$
$$I_{Q2(MAX\_SINK\_PK)} > f(n, D, F_{SW}, I_{OP}, I_{OS}, L_k) \quad (52)$$

At low duty cycles, the limiting factor will typically be the RMS rating, whereas at high duty cycles it would normally be the peak current limit of the MOSFETs.

In addition to the MOSFETs limitation, as the converter overall load current increases, the transformer magnetizing current $I_{M\_MAX}$ will also increase, eventually reaching the transformer saturation current limit (Figure 45).

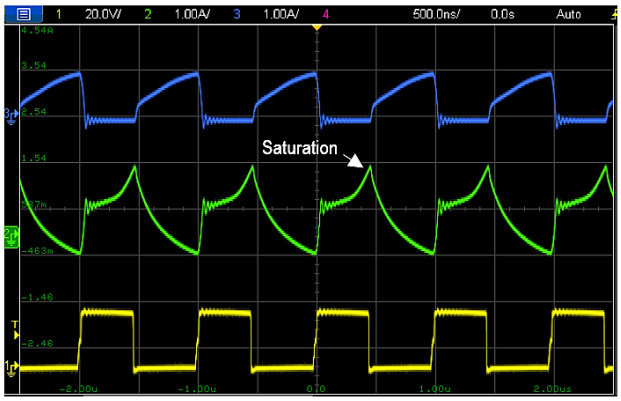


*Figure 45: Transformer at onset of saturation ($V_{SW}$ (), $I_P$ (), $I_S$ ())*

Care should be taken to verify experimentally the limits at full-load and at maximum expected ambient temperature, since the saturation current rating of the transformer decreases as the operating temperature increases, especially for ferrite-based cores.

Transformer temperature rise due to power loss in windings and core will also pose a practical limit to the effective rated current ($I_{LR}$).

$$I_{LR} > I_{P\_RMS} + I_{S\_RMS} \quad (53)$$

It is important to understand that the rated current value given in the datasheet is a DC current value causing a determined temperature rise, typically 40°C. Therefore, it does not consider the self-heating caused by AC losses, like hysteresis and eddy currents losses in the magnetic core, which are dependent on switching frequency as well as core material and volume, and it does not include the effect of winding ohmic losses due to AC resistance either (e.g. skin and proximity effects). For this reason, careful thermal validation of the transformer in the final prototype is essential.

Additional parameters limiting the practical output power are the minimum input voltage and the targeted isolated output voltage regulation, which as shown in previous sections, considerably worsens at higher load current on the isolated output(s).

Which one of these limitations comes into play first will depend on the particular component selection and converter operating conditions.

Note that solutions with external MOSFETs are rarely implemented in this topology due to the additional complexity, size and cost for the low power levels required.

### 4.3 Important PCB Layout Considerations

PCB Layout considerations for the buck converter with isolated output(s) are similar to a standard synchronous buck converter, albeit with important considerations regarding the converter 'hot' current loops.

A 'hot' loop is a circuit loop with very low inductance involving mainly capacitor(s) and switching devices, and with a pulsating current circulating in it. During the switching transitions, the low inductance allows very high di / dt in the loop, which together with the pulsating current, can easily cause EMI issues.

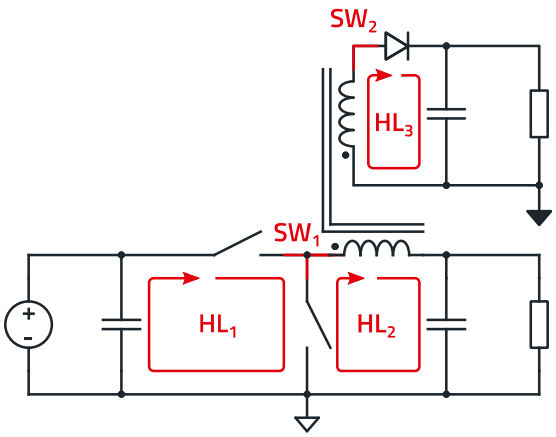


*Figure 46: Hot-loops and SW nodes of Isolated Buck Converter*

It is important to minimize the loop area enclosed by the current in a 'hot' loop, on the one side in order to minimize the parasitic magnetic field energy as well as radiation and noise pick-up capability by the loop. On the other side, in order to reduce the quality factor of the resonant RLC loop network, which may help to reduce any parasitic ringing generated during the switching transitions.

In a standard buck converter, there is one 'hot' loop enclosing the input capacitor and the two MOSFETs ($Q_1$ and $Q_2$). After adding one isolated output, three 'hot' loops with pulsating AC current and high di / dt are formed (Figure 46).

The reason for this is that the primary winding current reflected to the secondary side during the off-time (sourced by $C_{OP}$) does not 'see' the magnetizing inductance $L_M$, since current transformer action is taking place. The transformer leakage inductance is the only di / dt 'brake' available, but since its value is minimized for better voltage regulation and higher efficiency, a very high di / dt still can appear on switching transitions. Therefore, the area enclosed by the current in these 'hot' loops should also be minimized.

Note that an additional SW node in the isolated side is also created. As in a standard buck converter, the SW node traces must be kept as small and short as possible and far away from noise-sensitive traces.

## 5. STEP-BY-STEP DESIGN EXAMPLE

A design example is provided in this section along with experimental results, showing a typical design procedure.

### 5.1 Design Specifications

The main design specifications are as follows:

- $V_{IN}$ = 18 - 32 V (24 V nom.)
- $V_{OP}$ = 5.1 V ±2%
- $V_{OS}$ = 4.5 V to 5 V (balanced load)
- $V_{OS}$ = 4.2 V to 5.2 V (unbalanced load)
- $I_{OP\_MAX} = I_{OS\_MAX}$ = 0.3 A
- $P_{O\_MAX}$ = 3 W
- Focus on compact size
- Example applications are isolated multichannel communication interfaces and data acquisition systems powering transceivers, level-shifters, serial/deserializers, digital isolators, opto-couplers, etc.

### 5.2 Step-by-step Design Procedure

The converter will be implemented with a Buck topology, since for the target application, the non-isolated primary output rail is also used and needs to be of the same polarity than the input voltage rail. The duty cycle range is:

$$D_{MIN} = \frac{V_{OP}}{V_{IN\_MAX}} = \frac{5}{32} \approx 0.16 \quad (54)$$

$$D_{NOM} = \frac{V_{OP}}{V_{IN\_NOM}} = \frac{5}{24} \approx 0.21 \quad (55)$$

$$D_{MAX} = \frac{V_{OP}}{V_{IN\_MIN}} = \frac{5}{18} \approx 0.28 \quad (56)$$

The switching frequency is selected for a trade-off between power efficiency and solution size. In this case, it is set to $F_{SW}$ = 500 kHz. Due to the low output power requirement, and since only one isolated output is needed and a compact size is important in this case, a coupled-inductor will be used with a 1 : 1 turns ratio instead of a transformer (based on Würth Elektronik's catalog classification).

### 5.3. Coupled Inductor Selection

The magnetizing peak-to-peak ripple current value, limited to 40% of the combined full-load current is:

$$\Delta I_{M\_MAX} = 0.4 \cdot (I_{OP} + I_{OS}) = 0.24\ A \quad (57)$$

The required magnetizing inductance at nominal $V_{IN}$ is calculated as:

$$L_M > \frac{(V_{IN\_NOM} - V_{OP}) \cdot D_{NOM}}{\Delta I_{M\_MAX} \cdot F_{SW}} \approx 33\ \mu H \qquad (58)$$

The TDC-HV 8038 76889440330 from Würth Elektronik is selected. With a magnetizing inductance of 33 µH, it features rated current of 0.85 A (ΔT = 40°C) and saturation current of 1.85 A, and provides isolation voltage of 2 kV AC in a compact package of 8 mm × 8 mm × 3.2 mm (L × W × H). The Inductance vs Current curve for the TDC-HV 76889440330 is shown in Figure 47.

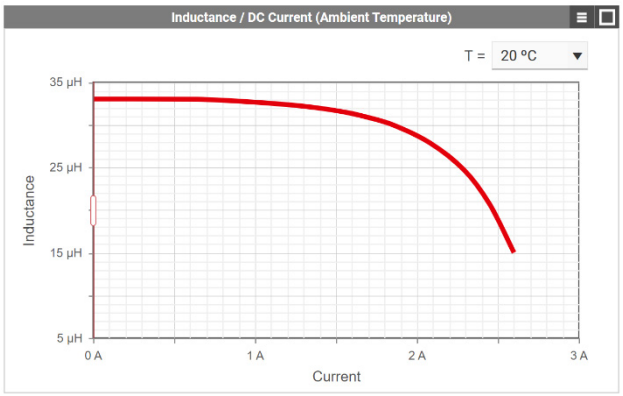


*Figure 47: Inductance vs Current TDC-HV 76889440330 (REDEXPERT)*

Note again that the rated current value corresponds to DC current in one winding only. Winding RMS currents at full-load are 0.37 A for primary winding and 0.35 A for secondary winding, resulting in an equivalent 0.72 Arms (measured via SPICE simulation). This provides a margin to the rated 0.85 A to account for the additional self-heating caused by AC losses in the magnetic core and windings.

The maximum instantaneous magnetizing current will be:

$$I_{M(MAX)} = I_{OP} + I_{OS} + \frac{\Delta I_{L\_MAX}}{2} = 0.72\ A \qquad (59)$$

The LM25017 IC synchronous controller from Texas Instruments is selected, which features integrated MOSFETs and Constant On-time (COT) control technique, offering very fast transient response. It can handle up to 650 mA DC load current and an input voltage range of 7.5 to 48 V, which sufficiently meet the requirements of the design. Based on LM25017 datasheet, the current limit of the high-side MOSFET is set, due to tolerances, in the range of 0.7 A to 1.3 A, with 1 A nominal.

The saturation current rating of the coupled-inductor should be higher than the worst-case current limit of 1.3 A, ideally with some margin to account for effects of temperature variations, which may be notorious in ferrite-based parts.

With this in mind, the 1.85 A rating of the TDC-HV will provide enough margin to the 1.3 A current limit. However, this should be again confirmed with experimental tests at the maximum expected ambient temperature.

### Input Capacitor ($C_{IN}$)

The input capacitance required for a maximum input ripple voltage of 0.5% of the nominal input voltage is (see (31)):

$$C_{IN} \approx \frac{0.21 \cdot 0.79}{0.005 \cdot 24\ V \cdot 500\ kHz} = 2.8\ \mu F$$

With the help of REDEXPERT, the WCAP-CSGP 885012209048 is selected (4.7 µF, 50 V, X7R, 1210, 10%). At a worst-case DC-Bias of 32 V, the capacitance will drop around 40%, to approximately 3.2 µF (Figure 48), whereas the ESR at 500 kHz is around 2.3 mΩ (negligible).

For better decoupling at high frequencies, the WCAP-CSGP 885012206121 (330 nF, 50 V, X7R, 0603, 10%) is added in parallel. The smaller package provides a higher self-resonance frequency.

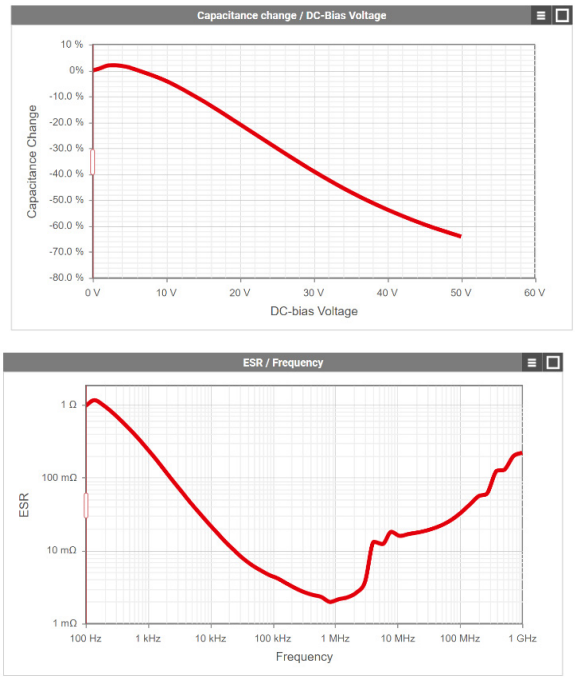


*Figure 48: WCAP-CSGP 885012209048 (REDEXPERT)*
*Top: Capacitance Change % vs $V_{DC}$-Bias Bottom: ESR vs Frequency*

### Output Capacitors ($C_{OP}$, $C_{OS}$)

The output capacitance on primary and secondary output rails is set so that to limit the voltage ripple to 1% of the primary output voltage. This is around 50 mV.

The initial values selected are (ESR ≈ 0):

$$C_{OP} = C_{OS} \approx 10\ \mu F$$

SPICE simulation with above values shows a maximum peak-to-peak voltage ripple of around 45 mV on the primary output and 28 mV on the secondary output, both below the maximum target of 50 mV.

The WCAP-CSGP 885012208019 is selected (22 µF, 10 V, X7R, 1206, 10%). At a DC-Bias of 5.5 V, the capacitance drops nearly 50% to 11 µF and the ESR at 500 kHz is again negligible of ~ 3 mΩ (Figure 49).

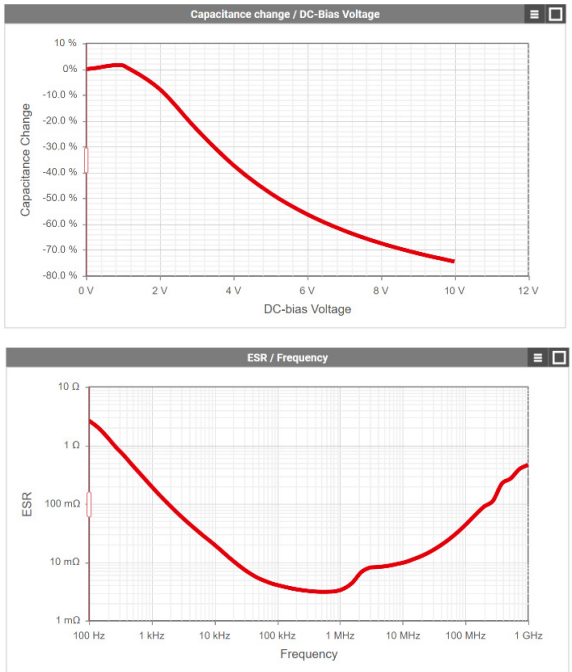


*Figure 49: WCAP-CSGP 885012208019 (REDEXPERT)*
*Top: Capacitance Change % vs $V_{DC}$-Bias Bottom: ESR vs Frequency*

### Rectifier Diode

Regarding the secondary diode, a very-low forward voltage drop and small size are important considerations. A Schottky rectifier diode type is therefore recommended. The SS1FN6 (60 V, 1 A) from Vishay has been selected for this design, encapsulated in a very small SMF package and featuring very low forward voltage drop $V_F$ of around 0.35 V (@ 25°C & 0.3 A). Such low $V_F$ is important in order to keep acceptable regulation of the isolated voltage rail. The maximum power dissipation is estimated at below 0.15 W, and with a junction-to-ambient thermal resistance of 125°C / W, the temperature rise is kept low to around 19°C. The designer can select an alternative part with similar characteristics from any preferred vendors.

## 5.3 LM25017 IC Controller Design

The datasheet of the LM25017 IC from Texas Instruments should be referenced in order to better understand the design steps which follow (see Figure 50).

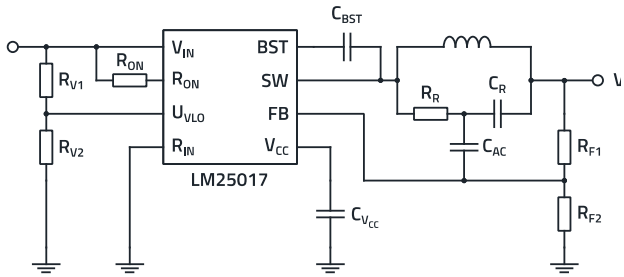


*Figure 50: LM25017 IC Circuit. Simplified Reference Schematic.*

### Undervoltage Lock-Out ($U_{VLO}$)

With $R_{V1}$ = 127 kΩ and $R_{V2}$ = 15.4 kΩ, the controller will turn on when the input voltage rises to 11.3 V with a hysteresis of 2.5 V, turning off at around 8.8 V, based on the formulae below.

$$V_{TH\_ON} = 1.225\ V \cdot \frac{R_{V1} + R_{V2}}{R_{V2}} = 11.3\ V \qquad (60)$$

$$V_{UVLO\_HYS} = 20\ \mu A \cdot R_{V1} = 2.5\ V \qquad (61)$$

### Setting the output voltage ($V_{OP}$)

With $R_{F1}$ = 4.7 kΩ and $R_{F2}$ = 1.5 kΩ, the regulated primary output voltage is set to around 5.1 V.

$$V_{OP} = 1.225\ V \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \approx 5.1\ V \qquad (62$$

**Setting the switching frequency ($F_{SW}$)**

With $R_{ON}$ = 120 kΩ a switching frequency of around 470 kHz is set:

$$R_{ON} = \frac{V_{OP}}{F_{SW} \cdot 9 \cdot 10^{-11}} = 120\ k\Omega \quad (63)$$

**Selecting Bootstrap and $V_{CC}$ capacitors**

Based on datasheet recommendation, the values initially selected are:

$$C_{BST} = 10\ nF \quad C_{V_{CC}} = 1\ \mu F$$

The WCAP-CSGP 885012206065 (10 nF, 25 V, X7R, 0603, 10%) and WCAP-CSGP 885012207023 (1.5 µF, 10 V, X7R, 0805, 10%) are selected for bootstrap and $V_{CC}$, respectively. DC-Bias effects are negligible in this case.

**Designing the Ripple Feedback Network ($R_R$, $C_R$, $C_{AC}$)**

Hysteretic-based controllers like the LM25017 require a ripple voltage in phase with the inductor current for regulation. Some techniques take the ESR voltage ripple on the output capacitor or use a discrete series resistor and then feed this signal to the controller feedback (FB) node. Note that in such cases, the resistive ripple must dominate over the capacitive ripple, which is out of phase with the inductor current. This can be achieved, but with the drawback of higher output voltage ripple amplitude, which may be unacceptable for some applications. A type-3 ripple network as shown in Figure 50 formed by $R_R$, $C_R$ and $C_{AC}$ generates the ripple signal artificially and thus independent of the output voltage ripple.

With the time constant $\tau = R_R \cdot C_R$ set higher than the switching period $T_{SW}$, $C_R$ integrates the current through $R_R$, which is proportional to the voltage across the inductor. This generates a voltage rising slope across $C_R$ during the on-time, and a falling slope during the off-time, resulting in a triangular waveform in phase with the inductor current. The generated ripple amplitude can be adjusted as follows:

$$\Delta V_{R\_MIN} = \frac{(V_{IN\_MIN} - V_{OP}) \cdot T_{ON(@V_{IN\_MIN})}}{R_R \cdot C_R} \quad (64)$$

The impedance of $C_R$ at the switching frequency should be much lower than the equivalent AC impedance of the paralleled feedback resistors. In this case, it is set to at least 10 times lower.

$$C_R \geq \frac{5 \cdot (R_{F1} + R_{F2})}{\pi \cdot f_{SW} \cdot R_{F1} \cdot R_{F2}} = 3\ nF \quad (65)$$

It is selected $C_R$ = 4.7 nF using WCAP-CSGP 885012206087 (4.7 nF, 50 V, X7R, 0603, 10%).

The charging resistor value $R_R$ is initially calculated for a worst-case minimum ripple amplitude of 25 mV:

$$T_{ON(@V_{IN\_MIN})} = \frac{R_{ON} \cdot 10^{-10}}{V_{IN\_MIN}} = 670\ ns \quad (66)$$

$$R_R \leq \frac{13\ V \cdot 670\ ns}{25\ mV \cdot 4.7\ nF} = 73.4\ k\Omega \quad (67)$$

It is selected $R_R$ = 33 kΩ which provides a higher peak-to-peak minimum ripple amplitude of around 50 mV, making the feedback loop more robust against noise.

The AC coupling capacitor ($C_{AC}$) lets the AC ripple through onto the feedback node while blocking the DC level between the ripple node and the feedback node. For this, $C_{AC}$ should present much lower impedance at the switching frequency than $C_R$. In this case, at least 10 times lower impedance is considered:

$$C_{AC} \geq 10 \cdot C_R = 47\ nF \quad (68)$$

The AC coupling capacitor is implemented with a WCAP-CSGP 885012206095 (100 nF, 50 V, X7R, 0603, 10%).

**Minimum Load Resistor (Secondary Output)**

A minimum load resistor (a.k.a. pre-load resistor) is required on the isolated output in order to prevent $V_{OS}$ to increase at no-load condition, due to energy transfer from the leakage inductance to $C_{OS}$ each switching cycle. Its value must be adjusted experimentally, and it is a trade-off between efficiency and voltage regulation. In this case, a value of 300 Ω was selected.

### 5.4 Experimental Results

The PCB prototype is shown in Figure 51, and the most relevant experimental results are included in this section.

SW node and Winding Currents are shown in the Figure 52. Voltage Regulation, Isolated Output Regulation and Power Efficiency are shown in Figure 53, Figure 54 and Figure 55, respectively, while Figure 56 shows the worst-case component surface temperature.

For all the details and the complete experimental results please refer to the reference design document RD006.

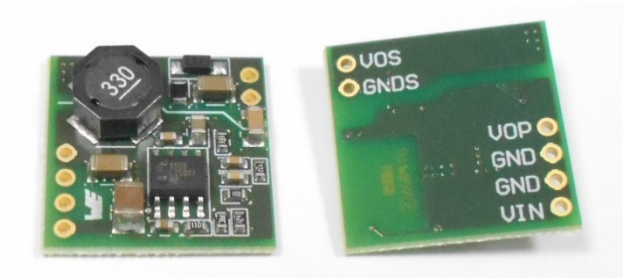


*Figure 51: Board Image (top and bottom sides view)*

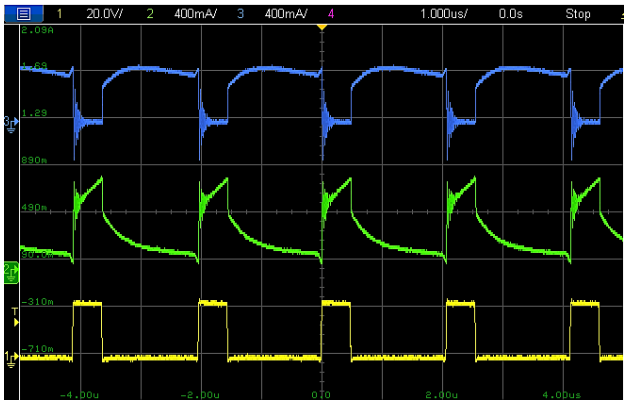

*Figure 52: Waveforms at full load (balanced) ($V_{SW}$ (), $I_P$ (), $I_S$ ())*

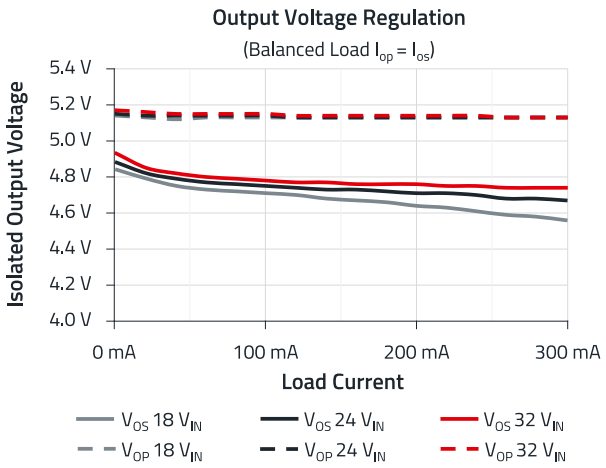


*Figure 53: Voltage Regulation @ $V_{IN}$ (balanced load: $I_{OP} = I_{OS}$)*

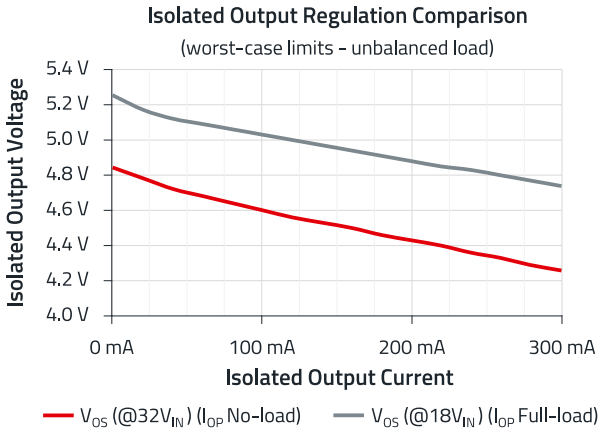


*Figure 54: Isolated Output Regulation – worst-case limits @ $V_{IN}$ (unbalanced load)*

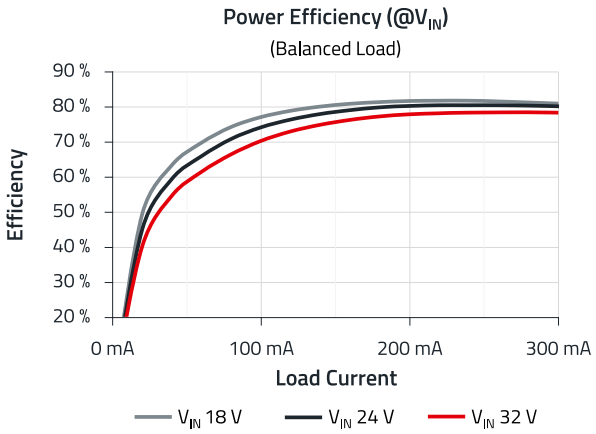


*Figure 55: Power Efficiency @ $V_{IN}$ (balanced load: $I_{OP} = I_{OS}$)*

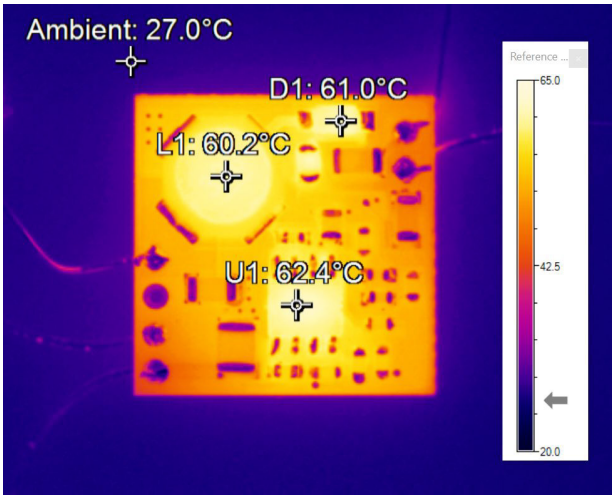


*Figure 56: Worst-case Component Surface Temperature ($V_{IN}$ = 32 V, $I_{OP} = I_{OS}$ = 0.3 A (full load, balanced))*

# 6. WÜRTH ELEKTRONIK MAGNETICS FOR BUCK CONVERTER WITH ISOLATED OUTPUTS

## 6.1 Coupled-Inductors

Virtually any of the coupled inductor series found in Würth Elektronik catalog can be used in the isolated buck converter topology, when only one secondary output is required. However, with the requirements of the most common target applications in mind, the following can be highlighted:

**TDC-HV (Tiny-Double-Coil – High-Voltage)**

- Inductance range: 5.6 – 33 µH
- Rated Current range: 0.85 – 1.4 Arms
- Saturation Current range: 1 – 4.7 A
- Isolation voltage: 2000 V (AC)
- Turns-ratio: 1:1
- Dimensions (L × W × H) (mm): 8018 (8 × 8 × 1.8) 8038 (8 × 8 × 3.8) – see Figure 57.

*Figure 57: TDC-HV 8018 (left) and 8038 (right)*

**DPC-HV (Double-Power-Coil – High-Voltage, see Figure 58)**

- Inductance range: 1 – 47 µH
- Rated Current range: 0.6 – 2.9 Arms
- Saturation Current range: 0.7 – 5 A
- Isolation voltage: 1500 V (AC)
- Turns-ratio: 1 : 1
- Dimensions (L × W × H): 5.2 × 5.2 × 3.1

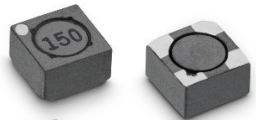

*Figure 58: DPC-HV Image*

**WE-MTCI (Multi-Turns Coupled Inductor, see Figure 59)**

- Inductance range: 10 – 33 µA
- Rated Current range: 0.6 – 0.95 Arms
- Saturation Current range: 0.75 – 1.5 A
- Isolation voltage: 800 V (AC)
- Turns-ratio: 1 : 1.5, 1 : 2, 1 : 3
- Dimensions (L × W × H): 5.2 × 5.2 × 3.1

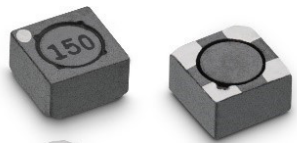

*Figure 59: WE-MTCI Image*

## 6.2 Custom Transformers Range

Würth Elektronik offers a wide selection of transformers for this topology featuring from one up to several isolated outputs: the WE-IBTI series. These custom-made transformers have been tailored and optimized for specific reference designs. Some of their features are as below:

- From 1 up to 4 secondary windings
- Different turns-ratios
- From 2.5 V up to 100 V input voltage range
- From 490 V up to 5 kV isolation

Please, contact the custom magnetics team at Würth Elektronik should you have special requirements for your application.

*Figure 60: Example of WE-IBTI Transformers*

## 6.3 Selecting a Transformer or a Coupled Inductor?

Based on Würth Elektronik portfolio, for applications requiring multiple isolated outputs obtained via independent windings, a transformer is currently the only choice. However, for applications requiring only one isolated output, the question commonly arises of whether to select a WE transformer or a WE coupled inductor. The answer typically lies on the specific requirements of the application.

If compliance with relevant standards requiring basic or reinforced insulation for a set working voltage is required, then a transformer should be used, since coupled inductors (at the time of this document) are offered only with functional insulation. For higher input voltages (typ. above 36 V), higher output current or power (typ. over 1 A and/or above 3.5 W) as well as higher dielectric insulation voltage ratings (over 2 kV), transformers would also be the choice. Coupled inductors are an optimal solution for lower power applications (typ. below 3.5 W) in which a compact size is paramount and where any electrical safety requirements are met by means of a separate magnetic component in the application or a specific isolation solution.

## 7. SUMMARY AND CONCLUSION

One or more galvanically isolated outputs can be easily obtained from a synchronous buck converter topology, simply by adding coupled windings to the power inductor and a peak rectifier circuit formed by a diode and a capacitor to each output. The output voltage on each isolated output would track the buck converter regulated output voltage scaled by the corresponding turns-ratio. The isolated rails are therefore only 'indirectly' regulated, and the parasitic elements of real components can easily degrade the voltage regulation of the isolated outputs. Considerations like a lower operating duty cycle, a lower switching frequency, lower parasitic resistances and/or lower leakage inductance of the transformer/coupled-inductor can all help to improve the voltage regulation. Alternative solutions are using a synchronous buck-boost power stage or adding post-regulation stages like LDOs or DC-DC micromodules to the output rails, especially in applications requiring very tight regulation.

In any case, the magnetic component plays a key role in achieving high efficiency, small size and good isolated voltage regulation in this topology. As a solution, Würth Elektronik provides a broad range of compact coupled-inductor series featuring optimal characteristics for the buck converter with isolated output(s) topology, in addition to many custom transformers which have been optimized for reference designs of leading semiconductor manufacturers. The validated reference design example provided in this application note illustrates a simplified step-by-step design procedure which can serve as a reference to the designer of low-voltage isolated auxiliary supplies.

# A APPENDIX

## A.1 Energy Analysis

In this appendix, an analysis of the energy flow in the buck converter with one isolated output is performed. Important differences compared to the standard buck converter will be shown. Note that, for the case of multiple isolated outputs, the same procedure can be applied and the calculations scaled for each additional isolated output added.

For the analysis, the time windows when the control transistor ($Q_1$) is conducting (on-time) and not conducting (off-time) will be considered separately, and the average net energy in the relevant components will be calculated in each of these time windows.

The average energy stored or delivered by a component within a set time window Δt is given by:

$$E_{\Delta t} = V_{AV\_\Delta t} \cdot I_{AV\_\Delta t} \cdot \Delta t \qquad (69)$$

where:

$E_{\Delta t}$: Net energy in component (+ stored) (- delivered)

$V_{AV\_\Delta t}$: Average Voltage across component during Δt

$I_{AV\_\Delta t}$: Average Current through component during Δt

### ON-Time Analysis

When the control transistor is turned on, energy is transferred from the input supply and input capacitor to the transformer, the primary output capacitor and the primary output load.

Based on reference schematic in Figure 61 and considering the waveforms depicted in previous Figure 13 and Figure 14, the net energy in the transformer is:

$$E_{L_{ON}} = (V_{IN} - V_{OP}) \cdot I_M \cdot D \cdot T_{SW} \qquad (70)$$

Referencing previous (2) and (21):

$$V_{IN} = \frac{V_{OP}}{D} \qquad I_M = I_{OP} + n \cdot I_{OS}$$

Substituting (2) and (21) in (70) and simplifying, we obtain:

$$E_{L_{ON}} = V_{OP} \cdot (I_{OP} + n \cdot I_{OS}) \cdot (1 - D) \cdot T_{SW} \qquad (71)$$

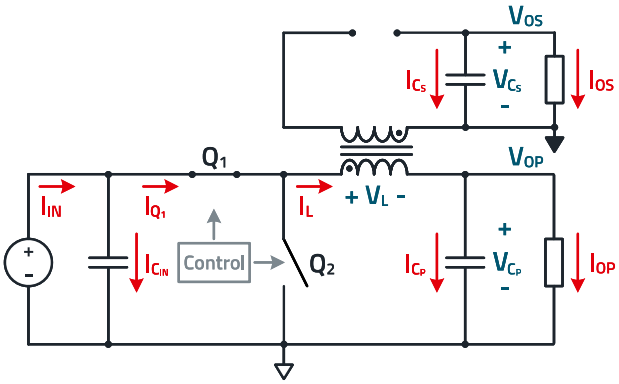


*Figure 61: Reference Schematic for on-time analysis*

This expression can be split into two terms:

$$E_{L_{ON}} = E_{L_{ON\_P}} + E_{L_{ON\_S}} \qquad (72)$$

where:

$$E_{L_{ON\_P}} = V_{OP} \cdot I_{OP} \cdot (1 - D) \cdot T_{SW} \qquad (73)$$

and,

$$E_{L_{ON\_S}} = n \cdot V_{OP} \cdot I_{OS} \cdot (1 - D) \cdot T_{SW} \qquad (74)$$

From previous (16), we have:

$$V_{OP} = \frac{V_{OS}}{n} \qquad (75)$$

Substituting in (74) and simplifying, we obtain:

$$E_{L_{ON\_S}} = V_{OS} \cdot I_{OS} \cdot (1 - D) \cdot T_{SW} \qquad (76)$$

From (73), it can be observed that $E_{L\_ON\_P}$ is the energy that the primary load needs during the OFF-time ($t_{OFF}$), with:

$$t_{OFF} = (1 - D) \cdot T_{SW} \qquad (77)$$

Similarly, $E_{L\_ON\_S}$ is the energy that the secondary (isolated) load needs during the off-time.

Since in steady-state operation, the delta energy in the transformer needs to be zero in a full switching period (volt-second balance), it can be confirmed that during the on-time window, the magnetizing inductance stores the same amount of energy which will be used to supply the output loads during the off-time.

But where is this energy coming from? Let's see next how it is actually coming from the input capacitor ($C_{IN}$).

The input supply current ($I_{IN}$) equals the average current through the control transistor $Q_1$ which is the magnetizing current multiplied by the duty-cycle, as below:

$$I_{Q1\_AV} = I_{IN} = I_M \cdot D \quad (78)$$

The average current through the input capacitor during the on-time equals the input supply current minus the magnetizing current (since $I_{Q1\_ON} = I_M$):

$$I_{C_{IN\_ON}} = I_{IN} - I_{Q1\_ON} = I_M \cdot (D - 1) \quad (79)$$

The above expression can be also written as:

$$I_{C_{IN\_ON}} = - I_M \cdot (1 - D) \quad (80)$$

The energy delivered from the input capacitor during the on-time is:

$$E_{C_{IN\_ON}} = V_{IN} \cdot I_{C_{IN\_ON}} \cdot D \cdot T_{SW} \quad (81)$$

and this yields, replacing $V_{IN}$ and $I_M$ based on previous (2) and (21):

$$E_{C_{IN\_ON}} = - V_{OP} \cdot (I_{OP} + n \cdot I_{OS}) \cdot (1 - D) \cdot T_{SW} \quad (82)$$

We can see that this equals (71), which gives the energy stored in the transformer during this on-time window. The negative sign in (82) indicates that the input capacitor is delivering this energy, whereas the positive sign in the transformer equation (71) means that the transformer is storing this energy.

With this, it can be seen how the input supply provides the energy for the primary output load plus the energy which is stored in the primary output capacitor ($C_{OP}$) during this on-time window. There is no energy transfer to the secondary side during the on-time, as the diode is reverse-biased and the secondary winding current is zero. The isolated output capacitor ($C_{OS}$) supplies the energy to the isolated output load during this on-time window.

It will be shown next that the energy stored in the primary output capacitor during the on-time window equals the energy being delivered by the secondary output capacitor to the isolated load during this same on-time window.

The average current though the primary capacitor during the on-time equals the magnetizing current minus the primary output current.

$$I_{C_{P\_ON}} = I_M - I_{OP} = n \cdot I_{OS} \quad (83)$$

And the net energy in $C_{OP}$ is:

$$E_{C_{P\_ON}} = n \cdot V_{OP} \cdot I_{OS} \cdot D \cdot T_{SW}$$
$$E_{C_{P\_ON}} = V_{OS} \cdot I_{OS} \cdot D \cdot T_{SW} \quad (84)$$

The net energy delivered by $C_{OS}$ in the on-time is:

$$E_{C_{S\_ON}} = - V_{OS} \cdot I_{OS} \cdot D \cdot T_{SW} \quad (85)$$

It can be observed how, during the on-time, the primary output capacitor stores the same amount of energy that the secondary output capacitor needs to supply the isolated load during the on-time, when no energy transfer to the secondary side is possible. In steady-state operation, the delta energy in a capacitor within a full switching cycle must be zero (charge balance), which confirms that the primary output capacitor delivers during the off-time the energy previously stored in the on-time window to the secondary side capacitor.

It can be noted that this energy is transferred during the off-time window in so-called 'Forward-mode', which means that energy is directly transferred from primary to secondary side by transfomer action without energy stored in the transformer core airgap. The source of this energy is the electric field of the primary output capacitor. Conversely, the energy stored in the transformer during the on-time is transferred in so-called 'Flyback-mode', which means that energy is stored in the magnetic field in the core airgap during one part of the switching period (on-time window), and delivered during the other part (off-time window).

**OFF-time Analysis**

Since in a full switching cycle the delta energy in reactive circuit components, like transformer magnetizing inductance and capacitors must be zero, it is not necessary to make a full analysis of the off-time window again. The components which stored net energy during the on-time window ($L_M$ and $C_{OP}$) will now deliver that same energy during the off-time. And similarly, the components which delivered energy during the on-time ($C_{IN}$ and $C_{OS}$), will have to store that same amount of energy during the off-time.

So, during the off-time the input DC supply will charge the input capacitor:

$$E_{C_{IN\_OFF}} = V_{OP} \cdot (I_{OP} + n \cdot I_{OS}) \cdot (1 - D) \cdot T_{SW} \quad (86)$$

and the primary output capacitor will discharge its on-time stored energy as it is transferred to the secondary-side output capacitor:

$$E_{C_{P\_OFF}} = - n \cdot V_{OP} \cdot I_{OS} \cdot D \cdot T_{SW} \quad (87)$$

$$E_{C_{S\_ON}} = n \cdot V_{OP} \cdot I_{OS} \cdot D \cdot T_{SW} \quad (88)$$

The transformer (magnetizing inductance) will also deliver its on-time stored energy to supply both output loads now during the off-time window:

$$E_{L_{OFF}} = - V_{OP} \cdot (I_{OP} + n \cdot I_{OS}) \cdot (1 - D) \cdot T_{SW} \quad (89)$$

This analysis helps to gain a deeper understanding into the converter operation and the very particular way the energy is transferred from input to output of the converter through the transformer in this topology, with the unusual combination of direct (forward-mode) and indirect (flyback-mode) mechanisms.

## A.2 WE Isolated Buck Experimentation Board

This is a configurable experimentation board of a buck converter with isolated output (see Figure 62) which has been used to obtain the results shown in Figure 16 to Figure 22. The board is only for internal use at Würth Elektronik.

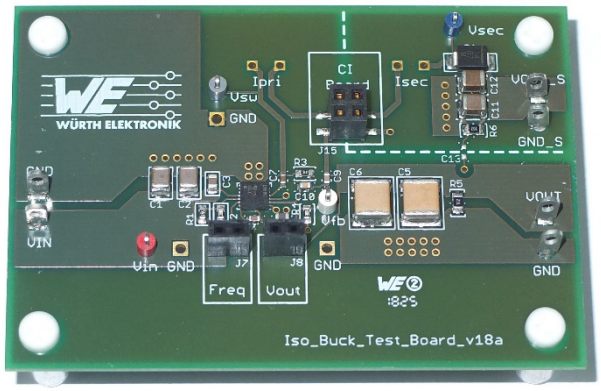


*Figure 62: Buck converter with isolated output (Experimentation Board)*

## A.3 Isolated Buck Evaluation Board

This is an evaluation board of a buck converter with isolated output (see Figure 63), which has been used to obtain the results shown in Figure 26 to Figure 29. The board is only for internal use at Würth Elektronik.

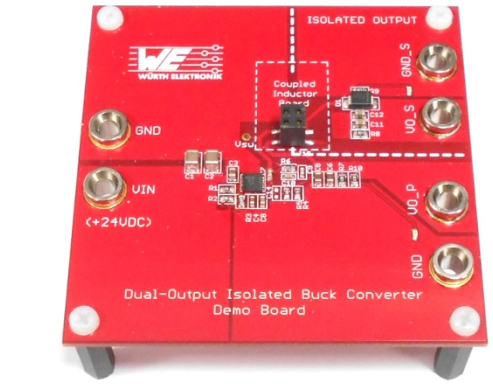


*Figure 63: Buck converter with isolated output (Evalboard with WE coupled inductor plug-in boards Detail)*

## IMPORTANT NOTICE

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| ANP017a | 2013/09/10 | Initial release of the application note |
| ANP017b | 2013/09/10 | Correction of Figure 1, page 1 |
| ANP017c | 2023/07/24 | Completely revised content, change from 8 pages to 29 |
| ANP017c | 2025/03/28 | Transferred to new graphical company template without any changes on the content |

***Note:*** *The current version of the document and the release date are indicated in the footer of each page of this document.*