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Designing An Ultra-Thin Stepdown Converter: Multiphase Vs. Multilevel

by Jianjing Wang, Efficient Power Conversion, El Segundo, Calif.

Over the past decade computers, displays, smart phones and other consumer electronics systems have become thinner while also becoming more powerful. As a result, the market continues to increase its demand for thinner power supply solutions with greater power density. This article examines the feasibility of adopting various nonisolated dc-dc stepdown topologies for an ultra-thin 48-V to 20-V, 250-W power solution.

After some comparison of several topology options, two of these converter topologies, namely the two-phase buck and the three-level buck, were selected for comparison. Converters based on these topologies were then designed, built and tested. GaN FETs were used in these designs to further reduce the converter size and improve efficiency beyond what could be achieved using silicon MOSFETs.

This article describes each design and evaluates the experimental results obtained in each case to determine which approach offers the optimal solution for this demanding application. The article begins by discussing the key design challenges that made the two-phase and three-level topologies the best candidates for this power supply application among the different options.

Design Challenges And Topologies

The bottleneck for thinning a stepdown converter mainly lies in the magnetic components. Designers usually have to either embed them into the circuit board,[1,2] or increase the switching frequency to shrink their size.[3,4] The former increases design and assembly complexity, while the latter requires advanced switching techniques to reduce switching loss, otherwise it incurs lower efficiency that leads to bigger thermal problems. These are the issues confronting the conventional synchronous buck converter.

A zero-voltage switching (ZVS) buck converter overcomes the loss issue at higher switching frequencies;[3,5] the major challenge with this topology is the control complexity.

But staying with the hard-switched approach, the multiphase converter, composed of multiple interleaved synchronous buck stages, allows the use of thinner inductors by distributing the output power processed by the single large inductor in the synchronous buck converter among multiple small inductors. This however may not address the efficiency loss and thermal issues of the inductors. As the volt-second for each inductor remains unchanged, higher inductance is required to keep the current ripple per phase within acceptable levels, otherwise high current ripple can lead to high losses.[6]

Another approach, the multilevel converter can achieve the same inductor current ripple as a synchronous buck converter with lower switching frequency and inductance.[7-9] This offers the benefits of reduced switching loss and inductor size. However, bootstrapping the high-side gate voltages and a comprehensive control scheme for start-up and flying capacitor voltage balancing can be challenging.

The hybrid synchronous buck converter combines a multilevel converter with a synchronous buck converter to improve efficiency and EMI performance.[10-11] Notably, unlike in the conventional multilevel converter, the effective frequency seen by the inductor is still the switching frequency, thus it is not as useful in shrinking the inductor size.

The inductor-less switched-capacitor converter removes the need of an inductor and, thus, is ideal for a thin design. The main issues are the lack of flexibility in stepdown voltage ratio, voltage regulation, and the design complexity when the number of voltage levels increases.[12]

This article will present the design of an ultra-thin 48-V to 20-V, 250-W converter using the two-phase and the three-level topologies, respectively. The design specifications are listed in Table 1. Both the electrical specifications and the component height restriction were dictated by the requirements of a gaming notebook application.

Table 1. Design specifications of the ultra-thin converter.

V_{IN}	V_{OUT}	I_{OUT}	Component height
44 to 60 V	20 V	12.5 A max	3.5 mm max

GaN FETs suited to each topology will be selected and used to improve the efficiency and power density.[13] The performance of these two topologies will be compared.

The Two-Phase Topology

The two-phase topology used to design an ultra-thin converter is shown in Fig. 1. The 100-V, 5.6-mΩ EPC2045[14] is selected for the four FETs. Texas Instruments' two-phase controller with integrated gate driver, the LM5143, is employed for control.

The inductors and the switching frequency are selected based on equation (1),

$$L = \frac{V_{IN} \cdot (1 - D) \cdot D}{f_{SW} \cdot \Delta I_L} \qquad (1)$$

where D is the duty cycle of Q1, f_{sw} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple.

Note that although the reduced current rating required for each inductor allows the use of a low-profile inductor, a higher inductance value is required to limit the current ripple and thus the inductor core loss. The 3.5-mm, 10-µH Vishay IHLP5050CE-01 inductor, along with the 400-kHz switching frequency, was chosen as it measures the lowest power loss. This inductance value keeps the current ripple at about 30% of the output current per phase, reducing the core losses compared to lower inductance values.

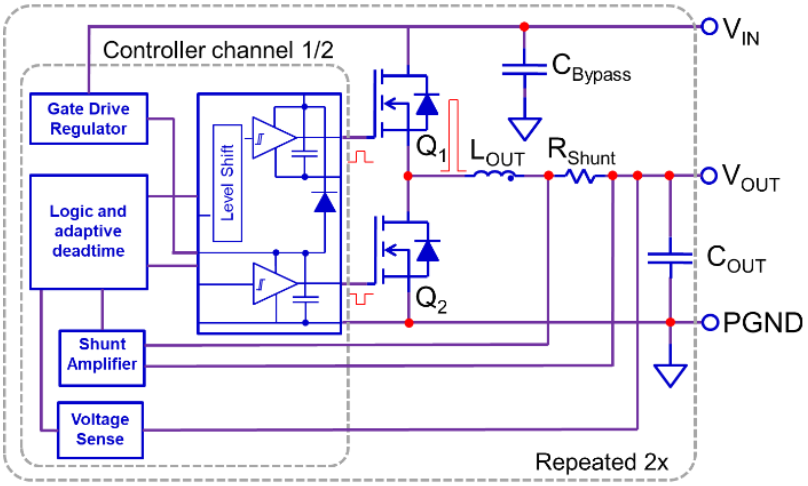

Fig. 1. Simplified schematic diagram of the two-phase converter.

The specifications and estimated loss[15] of the inductor are listed in Table 2. The inductors have high power dissipation and, it should be noted that further increasing the inductance in an effort to reduce the current ripple may help reduce inductor loss. However, with the height and current rating limitations, no such option was available using standard commercial inductor offerings at the time this design was implemented.

Table 2. Specifications and estimated losses of the inductors used in the two-level converter.

Part number	IHLP5050CE-01
Height	3.5 mm
Size	13.2 mm x 12.9 mm
DCR	30.4 mΩ
Estimated loss at full power*	3.7 W

*per phase for the two-phase converter.

This points out a limitation of using a multiphase topology for the ultra-thin power solution: although the required current rating for each inductor is reduced, the volt-second product remains unchanged. Therefore higher inductance is needed to maintain low core loss for each inductor.

The prototype of this two-phase converter is shown in Fig. 2. The two phases are designed to be as symmetrical as possible in order to avoid asymmetrical distribution of the current between them. All components are on the top side of the PCB, and the component height is limited to 3.5 mm.

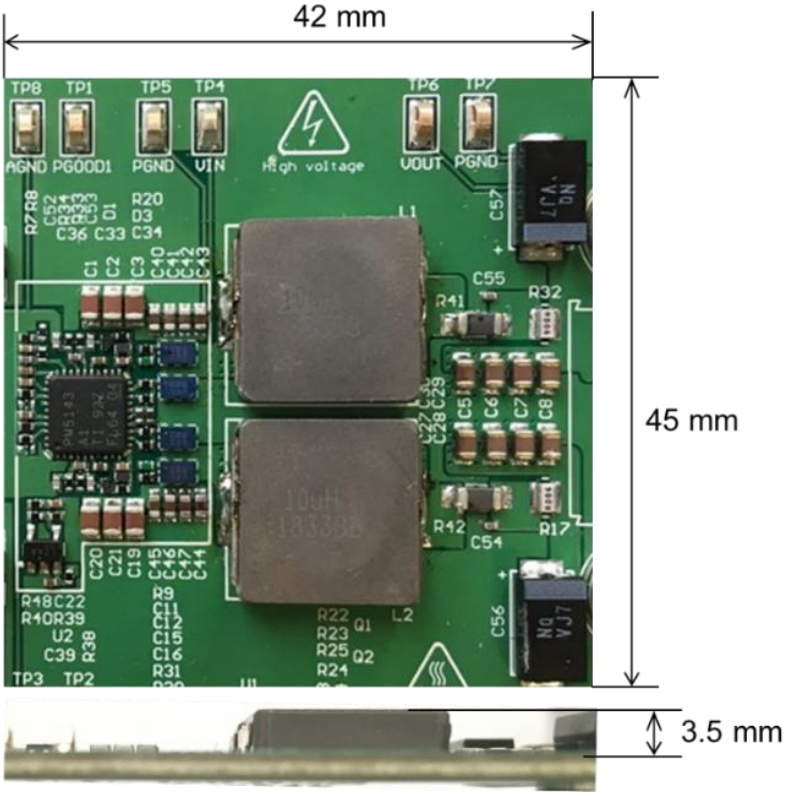

Fig. 2. A prototype of the 48-V to 20-V, 250-W GaN FET-based two-phase converter.

The Three-Level Topology

The three-level topology used to design an ultra-thin converter is shown in Fig. 3. The switching events at less than 50% duty cycle are shown in Fig. 4. Q1 and Q4 switching events are complementary, and so are the Q2 and Q3 pair.

Ideally, Q1 and Q2 have the same duty cycle and are 180 degrees phase shifted with respect to each other. During normal operation, the flying capacitor average voltage V_{FLY} is $1/2 \cdot V_{IN}$; all four FETs only need to block $1/2 \cdot V_{IN}$. This allows the use of FETs with a lower voltage rating, reducing the FET losses.

The 40-V, 2.8-mΩ EPC2055 that is of the same size as the 100-V EPC2045 in the two-phase converter is selected for Q2 through Q4. However, the 100-V, 2.8-mΩ EPC2218 is selected for Q1, as this FET needs to block the full input voltage for a short period during start-up.

The analysis of the switching events shows that the inductor sees twice the switching frequency. The relationship between the output inductance and the switching frequency is governed by:

$$L = \frac{V_{IN} \cdot (1 - 2D) \cdot D}{2 \cdot f_{SW} \cdot \Delta I_L}, D < 50\% \qquad (2)$$

where D is the duty cycle of Q1 and Q2.

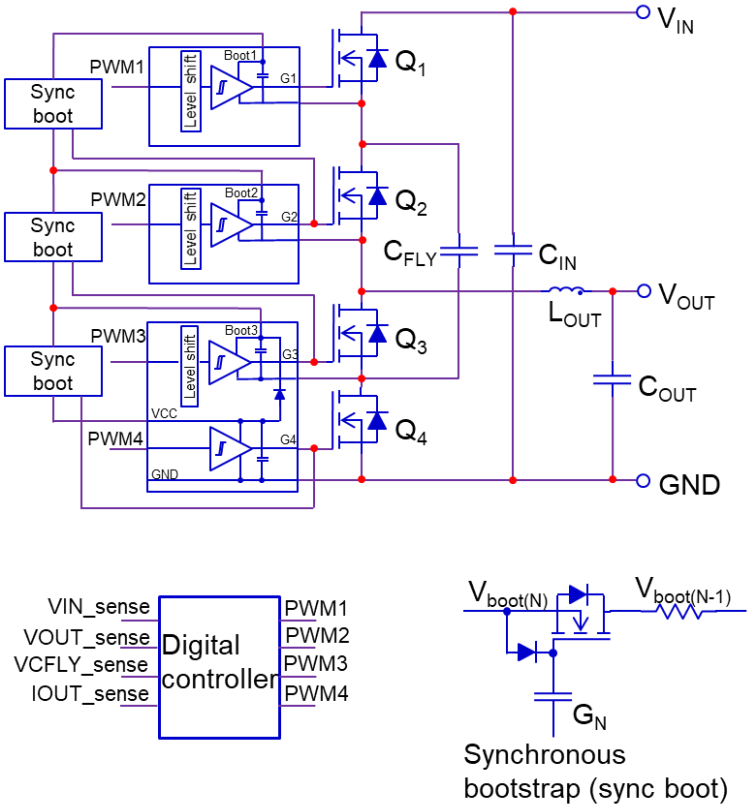

Fig. 3. Simplified schematic diagram of the three-level converter.

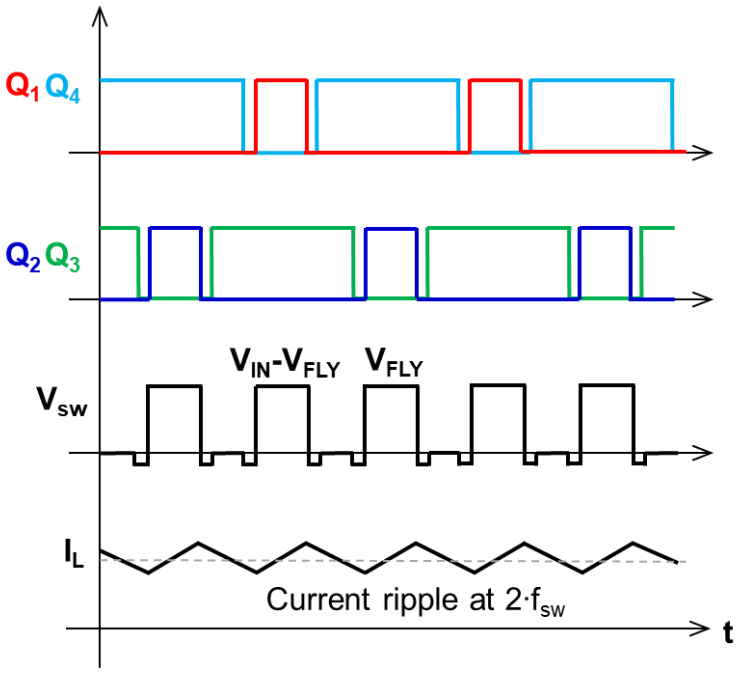

Fig. 4. Analytical switching events of the three-level dc-dc converter operating at D < 50%.

Compared to the conventional two-level synchronous buck converter, whose output inductance is given by equation (1), the inductance required by the three-level converter to achieve the same ΔI_L is much lower, facilitating the selection of a low-profile inductor. To compare it with the two-phase design, the same switching frequency 400 kHz and the same inductor height 3.5 mm are specified.

The 2.4-µH Würth 7443762504022 inductor is selected. Its specifications and estimated losses are listed in Table 3. This inductor has much lower power dissipation than the one used for the two-phase converter. What's more, the inductor losses are multiplied by two in the two-phase converter since it uses two inductors.

Table 3. Specifications and estimated losses of the inductor used in the three-level converter.

Part number	7443762504022
Height	3.5 mm
Size	18 mm x 25 mm
DCR	1.78 mΩ
Estimated loss at full power	1.5 W

In order to take full advantage of the lower FET voltage rating, it is imperative that the flying capacitor voltage be maintained at $1/2 \cdot V_{IN}$ to avoid overstressing any of the FETs, a process termed voltage balancing. The flying capacitor C_{FLY} must therefore ensure a reasonably small voltage ripple $\Delta V_{Cfly\_pk\text{-}pk}$ and the voltage and RMS current ratings as given in equations (3) through (5) respectively.

$$C_{FLY} \geq \frac{I_{OUT} \cdot D}{f_{SW} \cdot \Delta V_{Cflypk-pk}} \quad (3)$$

$$V_{rating} \geq 0.5 \cdot \left(V_{IN} + \Delta V_{Cflypk-pk}\right) \quad (4)$$

$$I_{rating} \geq I_{OUT} \cdot \sqrt{2 \cdot D} \cdot \sqrt{1 + \frac{1}{12}\left[\frac{V_{OUT} \cdot (0.5 - D)}{L \cdot f_{SW} \cdot I_{OUT}}\right]^2} \quad (5)$$

Considering that the capacitance of a ceramic capacitor decreases with the increase in the voltage across it,[16] six 2.2-µF, X5R, 50-V GRM188R61H225KE11D capacitors in parallel are used, effectively providing 2.2-µF capacitance at 24 V with greater than 12-A current carrying capability.

The fundamental control of the three-level converter needs to implement not only output voltage regulation, but also flying capacitor voltage balancing during normal operation and start-up. As there was no off-the-shelf three-level controller available when this converter was designed, the Microchip dsPIC33CK32MP102 digital signal controller was adopted for the digital control design. The control methodology is covered in reference.[17]

The prototype of the three-level converter is shown in Fig. 5. All components are on the top side of the board, and the maximum component height is 3.5 mm.

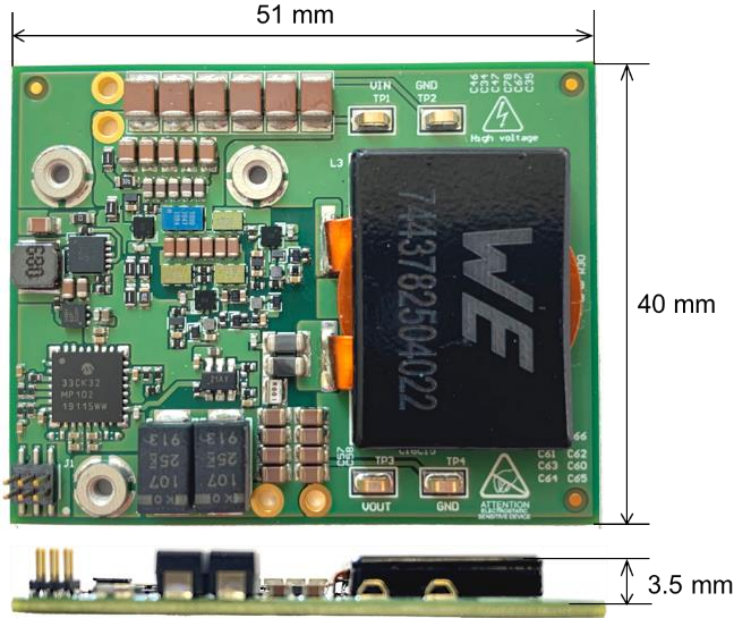

Fig. 5. Photo of the 48-V to 20-V, 250-W GaN FET-based three-level converter.

Performance Evaluation

The two converters, both designed to have the same height and power ratings, were tested. The switch-node waveforms of the two-phase and the three-level converter at 48 V to 20 V and a 12.5-A output are shown in Fig. 6.

Comparing the switch-node waveform of the three-level converter to that of the two-phase converter shows that it has double the frequency and duty cycle, and half the amplitude. The measured $\Delta V_{Cfly\_pk\text{-}pk}$ is 6 V; the value calculated by equation (3) is 5.9 V.

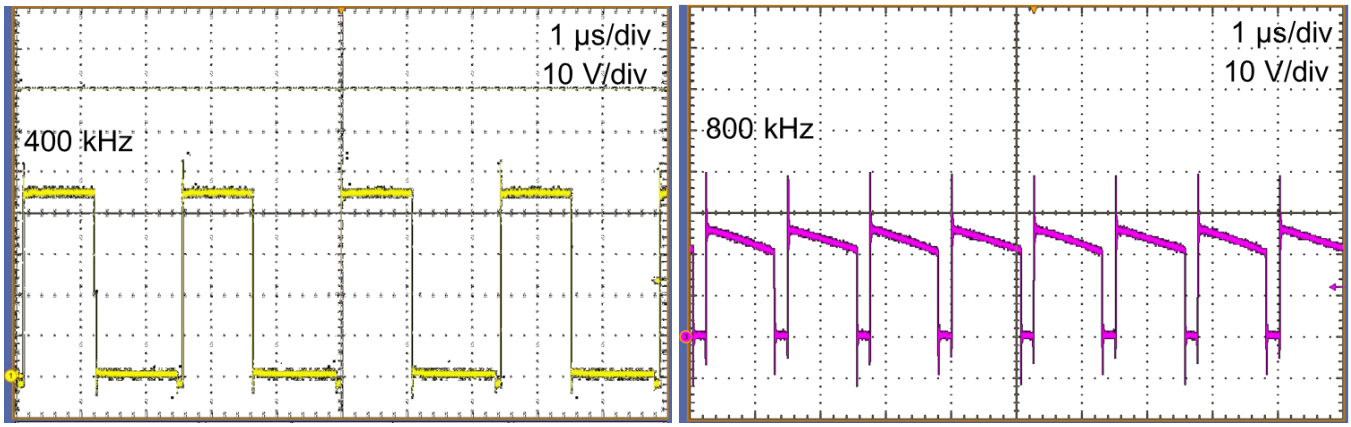

Fig. 6. Comparing the switch-node waverform of the two-phase converter (left) with that of the three-level converter (right), both obtained while stepping down 48 V to 20 V with a 12.5-A output current.

The overall power efficiencies of the two converters including the housekeeping power consumption at 48-V input and 20-V output are illustrated in Fig. 7. At the same 400-kHz switching frequency, the three-level converter is seen to achieve 98% peak efficiency and over 1% higher efficiency than the two-phase converter, which represents a 37% loss reduction at full load. This is because the three-level converter uses 40-V GaN FETs with lower $R_{DS(on)}$ and an inductor with substantially lower DCR. In addition, the core loss of the inductor is lower due to the higher effective inductor frequency and lower current ripple.

The thermal images of the two-phase and three-level converters operating at full power and with 800 LFM airflow are shown in Fig. 8. The three-level converter demonstrates lower temperature rise for all major components.

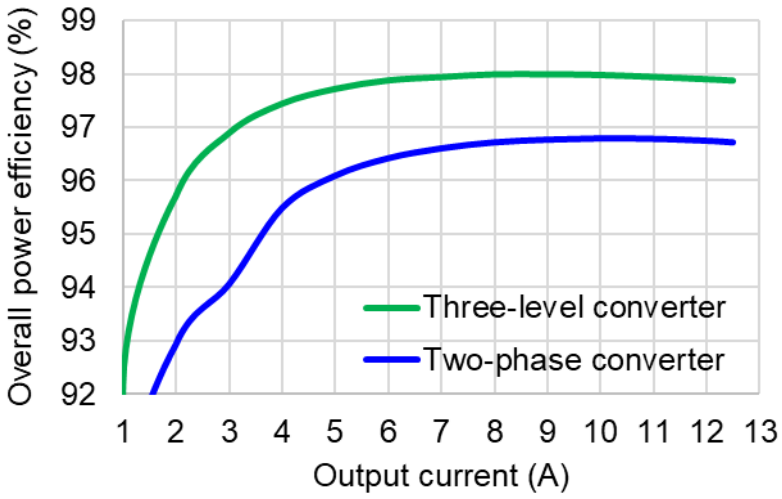

Fig. 7. Overall power efficiency of the three-level and two-phase converter at 48 V to 20 V.

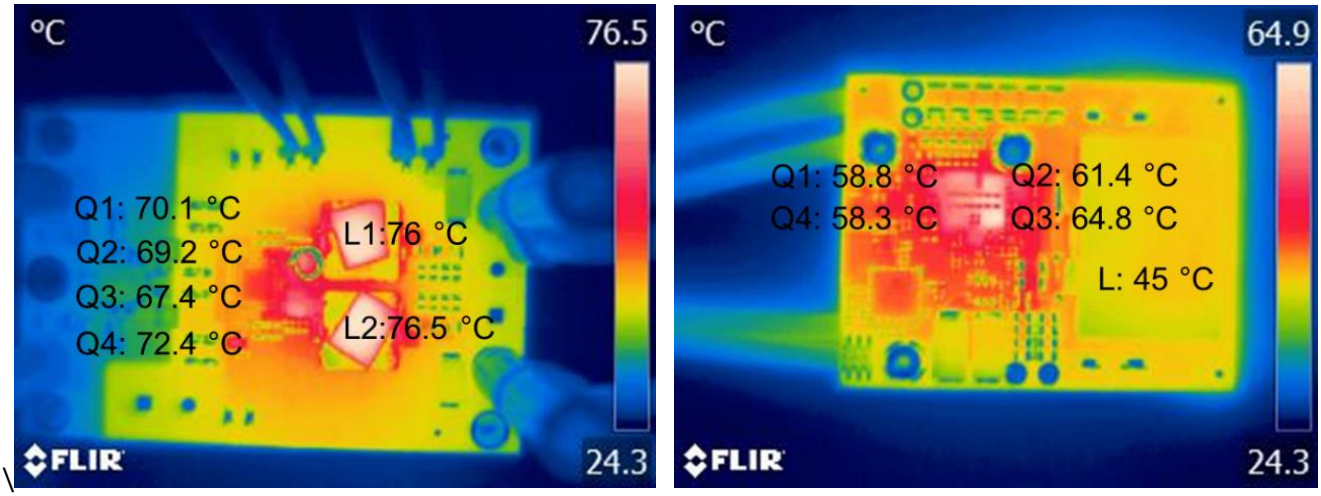

Fig. 8. Comparing the thermal performance of the two-phase converter (left) and the three-level converter (right) both tested at a 48-V to 20-V conversion and a 12.5-A output current. Measurements were taken after the components reached thermal steady state with 800-LFM airflow.

Conclusions

This article evaluated the design challenges and benefits of common dc-dc stepdown topologies for an ultra-thin 48-V to 20-V, 250-W converter. Two-phase and three-level power conversion topologies were selected to build buck converters with a maximum component thickness of 3.5 mm.

The three-level converter achieves a peak efficiency of 98% and is more efficient than the two-phase converter with the same height limitation and FET size. The multilevel topology allows the use of a thin inductor with low inductance value. The eGaN FETs not only reduce the area occupied with their tiny footprints, but also improve the overall power efficiency with their fast switching capability.

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About The Author

Jianjing Wang is a senior applications engineer at Efficient Power Conversion (EPC). Prior to joining the company in 2018, she was a senior engineer with ASTRI, Hong Kong from 2014 to 2015, and a research associate with the University of Bristol, UK from 2015 to 2018. Her experience includes power electronics packaging, active gate driving of GaN FETs, power device characterization, and designing various dc-dc converters.

Jianjing received her B.Eng. degree in control science and engineering from Huazhong University of Science and Technology, China in 2009, and the Ph.D. degree in power electronics from City University of Hong Kong, Hong Kong in 2014.

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