Application Note

Effective USB 3.1 filtering and protection

ANP007 // ROBERT SCHILLINGER // DR. RICHARD BLAKEY

1 Introduction

The USB connector and standard are one of the most widely implemented and successful interfaces ever used. The applications are commercial and industrial, and both have been pushing the standard to be faster. The USB standard has been updated to version 3.1. This standard increases data transfer speeds to 5 GBits/s (Gen 1) and 10 GBit/s (Gen 2). Higher data transfer speeds are required due to the ever-increasing resolution of media and network data rate requirements.

Increasing the data transfer speed means important parameters need to be considered, as this has implications in data transmission lines. Attenuating unwanted signals while maintaining the speed and integrity of data transfer is of paramount importance for EMI compatibility. For high-speed data lines, Würth Elektronik has common mode chokes for EMI suppression and TVS diodes for ESD protection. The WE-CNSW HF has been developed to attenuate common mode noise signals while maintaining signal integrity up to 10 GBit/s. For ESD protection, the WE-TVS is available with very low capacitances (< 0.6 pF) and is the ideal choice for higher frequencies. These components are also well suited for other high data transfer interfaces such as HDMI 4K, DisplayPort or GBit LAN.

This Application Note outlines the components needed to protect USB 3.1 devices and attenuate EMI that may cause the device to fail EMC testing. This will be demonstrated in USB Type-C dongle (Figure 1) to characterize the effectiveness of the components. For information and components suitable for USB 2.0, please refer to:

- ANP002 – The Protection of USB 2.0 Applications
- ANP024 – The USB Interface from EMC Point of View

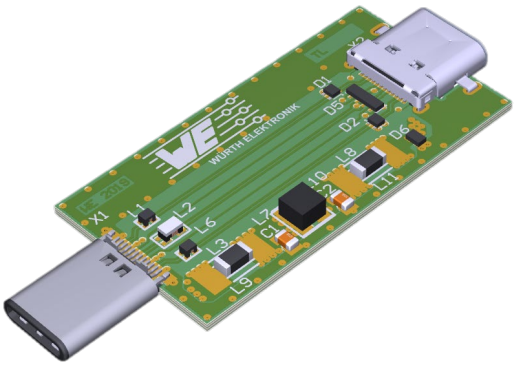

Figure 1: USB-C dongle used to demonstrate USB 3.1 filtering and protection

2 EMC considerations of symmetrical data lines

The USB interface is a bidirectional, symmetric interface (Figure 2).

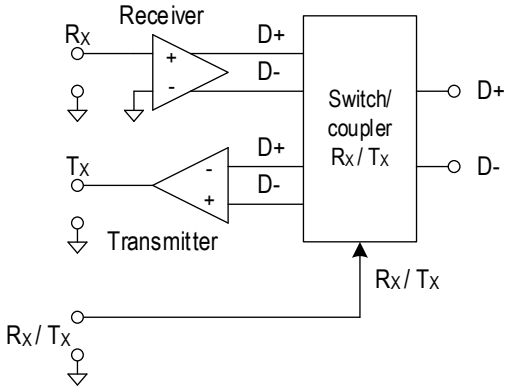

Figure 2: The USB interface is symmetrical and bidirectional

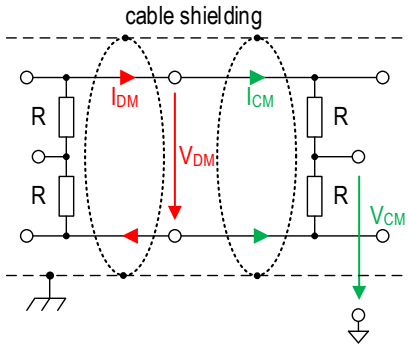

Figure 3: The symmetrical interface with its measurable interference voltages

V_{DM}, interference voltage between the signal wires, and V_{CM}, interference voltage between the voltage midpoint and the reference voltage (ground, cable shield), are both measurable. This means that both differential mode and common mode interference voltages can affect the USB transmission path. This can be interference from the interface itself or an electromagnetic effect from the environment in the form of inductive, capacitive or wave coupling.

2.1. Interference Emission

In the case of USB transmission, differential mode interference is mainly generated by non-linear signal harmonics due to impedance mismatching and inadequate circuit design. Asymmetry of the transmission path (e.g. transmitter, circuit board traces, conductor tracks, filters or cables) can lead to interference radiation and impairment of signal quality.

Common mode interference arises from parasitic coupling in the circuit environment of the USB controller. This is usually due to capacitive

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coupling on the USB signal with rising interference frequency and increasing amplitude. However, these interference types are found on both USB wires in phase and at the same amplitude and therefore the effect on the intended signal is reduced. Asymmetries in the cable or at the receiver often convert the originally common mode into a differential mode interference signal, however, which can then contribute to signal impairment (Figure 4).

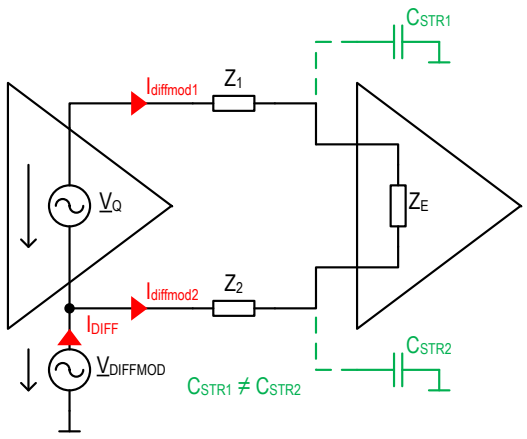

Figure 4: Conversion of differential mode to common mode interference due to parasitic coupling capacitances in the one channel of a differential pair

2.2. Interference immunity

Differential mode data transmission offers a significant advantage over the simple coaxial cable when it comes to the effect of interference on the USB. Depending on the shielding effectiveness of a coaxial cable, a transient, from a parallel mains cable for example, couples into the data line and interferes with the data signal (Figure 5). This leads to data or communication errors, which depend on the interference signal length and amplitude.

Symmetrical transmission techniques have numerous advantages including lower interference emission and higher interference immunity (Figure 3).

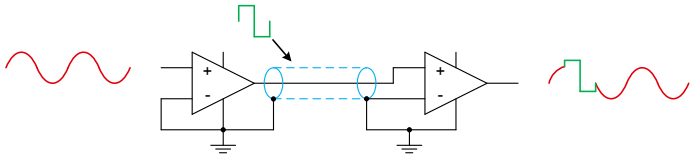

Figure 5: Effect of interference on a coaxial data transmission path

Figure 6 represents the case of differential mode data transmission with twisted pair wires. The polarity of the intended signal is reversed so that equal but opposite signals propagate. The signal difference is evaluated at the input of the receiver. The interference signal affects both wires in the same phase, so this cannot have an effect as an interference signal at the receiver.

Furthermore, in the case of the inductive interference effect (magnetic field), the twisting of the wires achieves compensation of the interference effect. Because of the symmetry of the partial inductances of the respective twisted wire, the interference influences compensate each other.

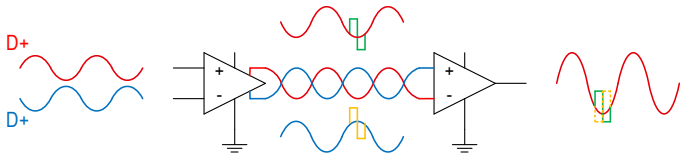

Figure 6: Compensation of electrical interference coupling of the differential mode signal input and twisted wire pairs

2.3. Possibilities of reducing emission and increasing interference immunity

It is apparent in practice that interference emissions cannot be completely prevented and, therefore, interference immunity has stringent requirements. The reason lies in many details, of which these are the most important:

- The inputs/outputs of the USB controller are insufficiently symmetrical; the USB signal displays common mode interference.
- The layout is not HF/EMC compatible, parasitic capacitances and the lack of wave impedance matching generate common mode interference.
- The circuit design (USB filter) is inadequate, the filters affect the signal quality and/or the insertion loss is too low.
- The interface design (receptacle, housing) is inadequate, poor ground reduces the shield attenuation of the cable, filters have poor ground reference.
- The USB cable is asymmetrical, poorly shielded, has inadequate ground connection. The cable deteriorates the signal quality, radiates signal harmonics and has insufficient shield attenuation towards external interference sources.

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2.4. Methods of reducing emission and increasing interference immunity

Common mode chokes (CMC) are fundamental for attenuating interference. Extremely low capacitances between the data line and ground are needed with USB 3.1. The values are strongly dependent on the properties of the CMC. The CMC must have a high degree of symmetry and low stray capacitance between the two windings. Furthermore, the ferrite permeability must have a low real part in the data signal frequency range, in order to reduce unwanted reflections at the CMC. The imaginary part of the permeability should be high within the frequency range to be filtered.

Transient interference signals, such as ESD and bursts, can generally be limited with varistors. Especially SMD multilayer varistors, which are particularly fast and withstand a high level of energy. However, their capacitance is generally too high, possibly corrupting the signal and definitely making them unsuitable for limiting transients in USB 3.1 data lines. Transient limitation with diodes is shown in Figure 7. Transients are limited against ground, both on D+ as well as on D- up to the forward voltage U_F of the diodes. This voltage is around 0.7 V for silicon diodes. A problem appears very quickly here, which is why the diode pair bellow has two red flashes: The signal voltage of the "mid-speed" signal is up to 2.8 V (D+ to D-), i.e. 1.4 V to ground. The positive branch must therefore be provided with an "offset" in order to avoid impairing higher signal voltages.

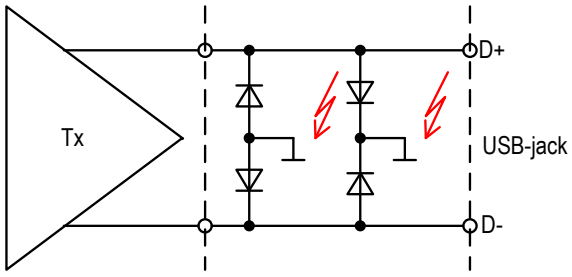

Figure 7: Diode array to reduce coupled transients (burst, ESD) on the USB interface

An additional TVS diode with a limitation voltage of 6 V sets the threshold value to approximately 6.7 V. This is sufficient protection, as TVS diodes with lower limitation voltages are too slow to limit ESD. The voltage levels are illustrated in Figure 9. Transient limitation at the connection of the supply voltage can be achieved at the same time using the additional diode D_5 in Figure 8. Although the capacitance of the TVS diode is low at 5 pF, it would be too high for USB 3.1. As V_{R1} is in series with D_3 and D_4, however, the capacitance of V_{R1} reduces the overall capacitance that affects the signal, as D_3 and D_4 have capacitances of approximately 2 pF. The capacitors are in series with D_3 and D_4 with reference to the signal, there is an overall signal-to-signal capacitive load of 2 pF and signal against ground of around 3 pF.

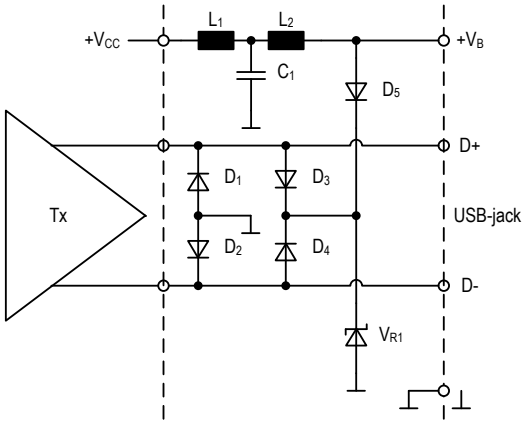

Figure 8: Diode array to reduce coupled transients (burst, ESD) on the USB interface with "offset" for higher signal levels

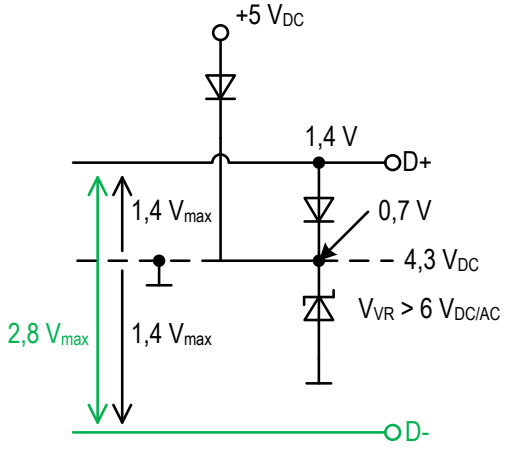

Figure 9: Voltage levels of the positive diode path

For the supply voltage, a low-pass π-filter with two ceramic capacitors and an inductor can be used (Figure 10). The current carrying capability is an important parameter, which is specified in the datasheets. The components should be selected to be adequate for the respective power output.

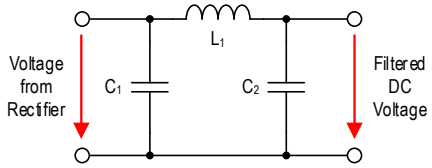

Figure 10: π-filter topology

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3 High frequency common mode chokes

Common mode chokes are inductors with two or more isolated windings. When a common mode signal passes through the component, magnetic flux accumulates in the core, resulting in high impedance at some frequencies. As differential signals cancel out the magnetic flux in the core, the impedance is low, allowing the signal to pass nearly un-attenuated.

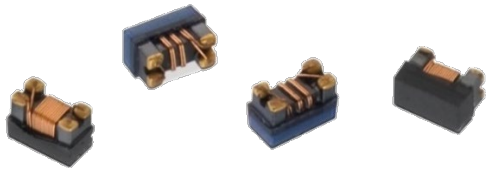

Figure 11: WE-CNSW HF

In Figure 12, the eye diagram for the **WE-CNSW** (left side) and the **WE-CNSW HF** (right side) is compared at 5 GBit/s. Both components have almost the same impedance in common mode (Figure 15). The main difference is in the differential mode impedance. The difference is big enough to see that the eye is smaller with the standard version.

At 2.5 GBit/s the difference is smaller (Figure 13). The harmonics of the signal are not filtered by the high frequency component nor the standard component.

The difference between the WE-CNSW and the WE-CNSW HF is not significant in the low frequency data range. Both will allow the data signal to pass as both WE-CNSW series are designed to have low differential impedance in this frequency range. However, a data signal with a higher frequency will be presented with higher levels of differential impedance. With the WE-CNSW, the cut-off frequency is about 2 GHz, whereas with the WE-CNSW HF the cut-off frequency is much higher, while still having the same impedance for common mode signals. At a data rate of 7 GBit/s the WE-CNSW also attenuates the base frequency of the signal while the WE-CNSW HF only attenuates the high frequency harmonics resulting in a passed eye diagram test (Figure 14).

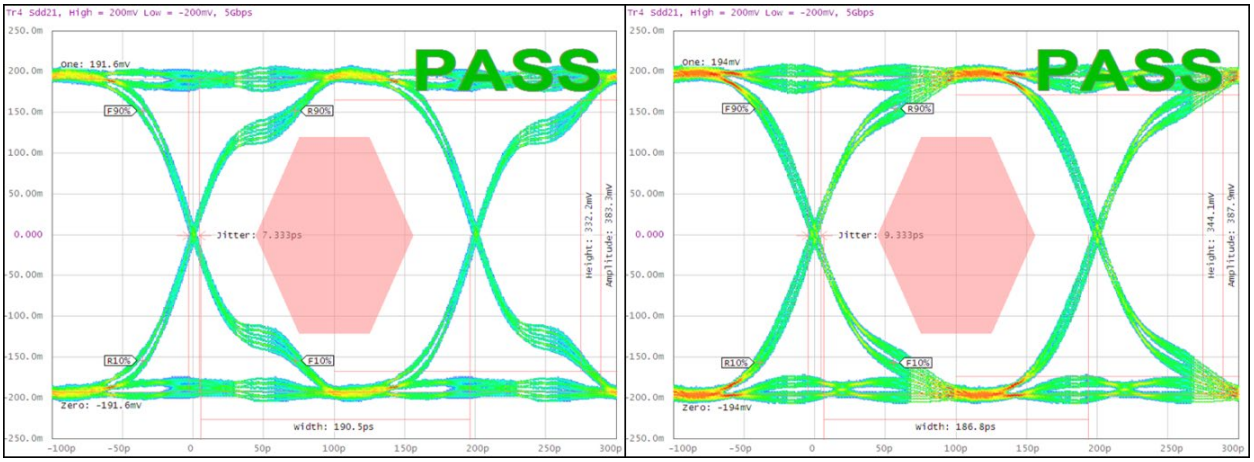

Figure 12: Eye diagram with the WE-CNSW filter (left) and the WE-CNSW HF filter (right) at 5 GBit/s

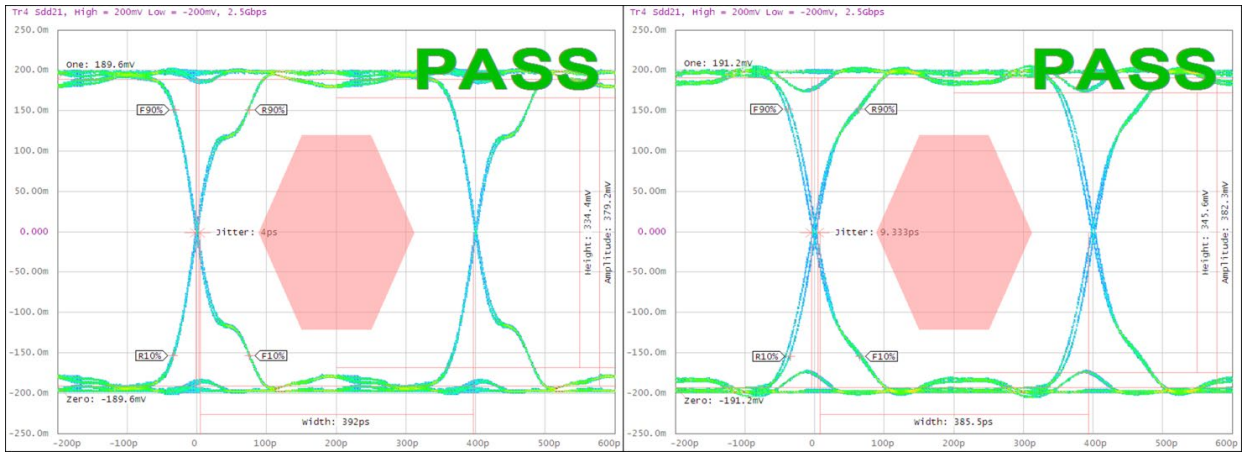

Figure 13: Eye diagram with the WE-CNSW filter (left) and the WE-CNSW HF filter (right) at 2.5 GBit/s

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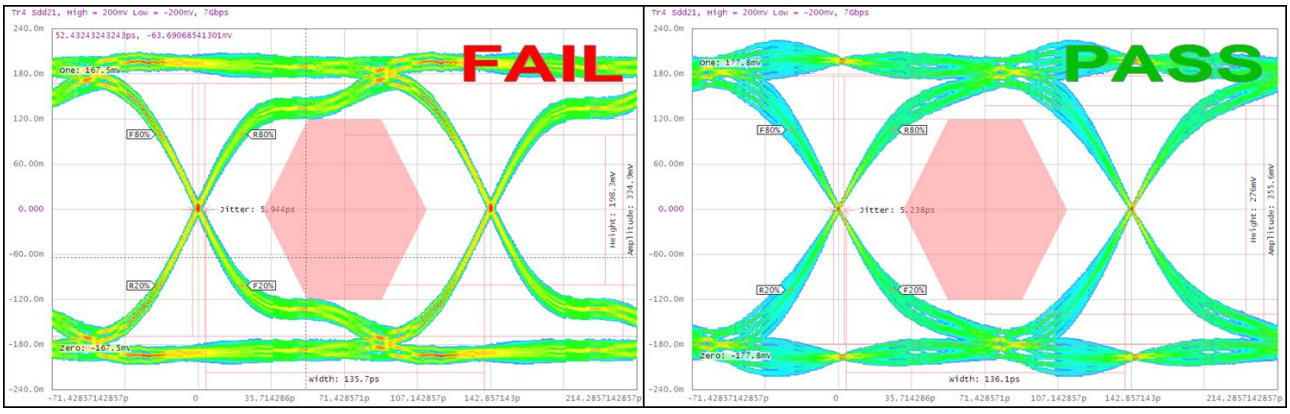

Figure 14: Eye diagram with the WE-CNSW filter (left) and the WE-CNSW HF filter (right) at 7 GBit/s

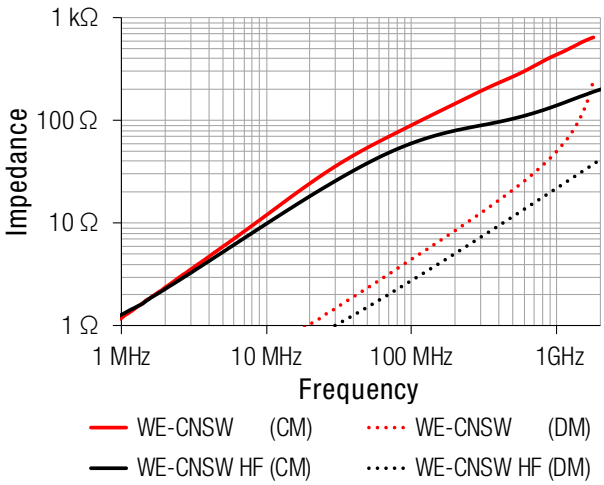

Figure 15: Comparison between the common and differential mode impedance of the WE-CNSW (744 231 091) and the WE-CNSW HF (744 233 56 00)

4 Transient voltage suppression (TVS) diodes

Due to their construction, modern semiconductors are fabricated with extremely small tolerance to high voltages. Integrated ESD protection normally works up to 500 V, but higher tolerance is needed in most applications to ensure stable and long-term functionality.

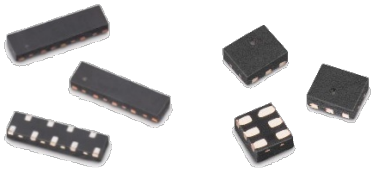

Figure 16: WE-TVS Super Speed Series

Würth Elektronik has launched the high frequency TVS diodes array series called **WE-TVS Super Speed Series**. These TVS diode arrays protect against ESD pulses according to EN 61000-4-2. Due to their ultra-low capacitance (< 0.6 pF) they are nearly invisible to high bit rate data such as USB 3.1, HDMI 2.0 and GBit Ethernet.

Additionally, the WE-TVS High Speed Series are high performance TVS diode arrays that include surge rated diodes. They are an excellent choice to protect high-speed data lines, like USB 2.0, VGA and Ethernet. The **WE-TVS High Speed Series** exceeds the requirements outlined in EN 61000-4-2. Due to their ultra-low capacitance (< 2.0 pF) they are nearly invisible on the signal lines.

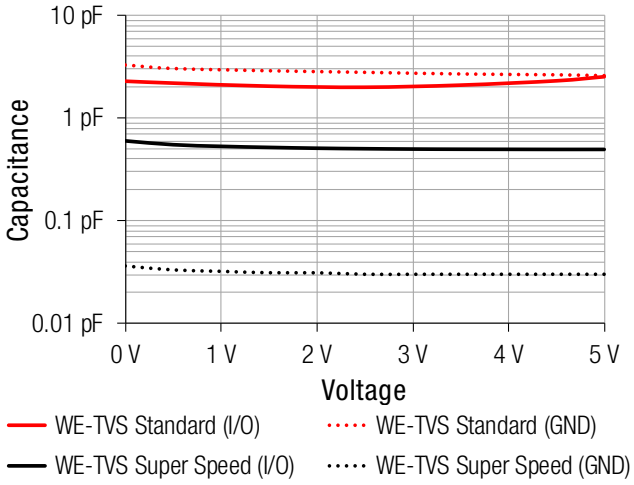

Figure 17: Comparison of the inter-pin capacitance between the WE-TVS High Speed Series (82400152) and the WE-TVS Super Speed Series (824014885)

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5 USB-Typ-C-Dongle

Modern demands have been pushing for a universal bus (USB) to be smaller, thinner and lighter. The USB Type-C connector was developed in parallel with the USB 3.1 standard (SuperSpeed+, USB 3.1 Gen 2), which is the updated standard of USB 3.0 (now USB 3.1 Gen 1). The connector now includes 24 pins (Figure 13) which include four power/ground pairs, two differential pairs (non-SuperSpeed+) and four SuperSpeed+ pairs (two used for USB 3.1). USB Type-C has data rates of up to 10 Gbit/s using one SuperSpeed+ and two SuperSpeed line pairs and can carry up to 5 A (100 W). To maintain signal integrity at these speeds, the capacitance of ESD devices must be even lower than that for USB 2.0 while CMCs need to present impedance to differential mode noise at higher frequencies.

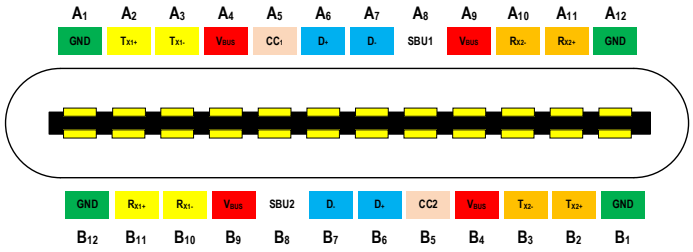

Figure 18: USB Type-C pin layout

From the above pin layout, the power pairs are A_1/A_4, A_9/A_{12}, B_1/B_4 and B_9/B_{12}, the SuperSpeed+ pairs $A_2/A_3/B_{10}/B_{11}$ and $A_{10}/A_{11}/B_2/B_3$ and the non-SuperSpeed+ A_6/A_7 and B_6/B_7. These three functions can be treated separately and the necessary protection and filtering can be seen below (Figure 19).

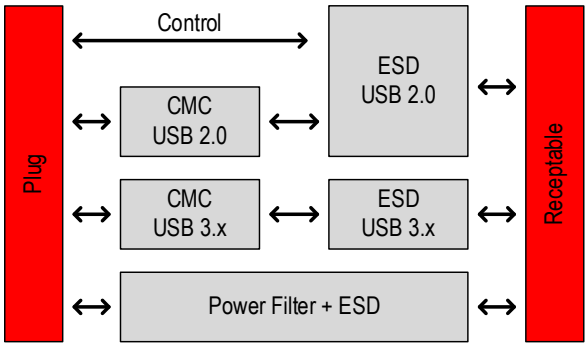

Figure 19: Block diagram of the USB Type-C dongle

Additionally, A_5/B_5 are used to detect the connection and configure the interface. A_8/B_8 can be used for audio or additional features that have yet to be designated.

The nominal differential impedance of USB 3.1 data lines is 90 Ω, which must be maintained in the differential microstrip of the dongle. Z_0 is calculated using the standard microstrip formula (1). To achieve impedance matching, the trace width w and height t, the trace separation distance s of the differential data traces in addition to the PCB permittivity and thickness h must be considered (Equation 2).

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98\,h}{(0.8\,w + t)}\right] \quad (1)$$

$$Z_{diff} = 2 \cdot Z_0 \cdot \left[1 - 0{,}48 \cdot e^{\left(-0{,}96 \cdot \frac{s}{h}\right)}\right] \quad (2)$$

The calculated parameters were implemented as seen below (Figure 20).

Figure 20: Trace dimensions and PCB layer stack to attain 90 Ω line impedance. (w = 220 µm, s = 150 µm, h = 177 µm)

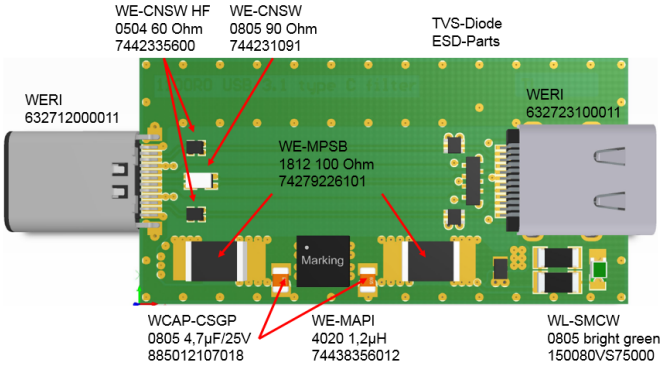

Figure 21: Visualization of the USB dongle

5.1. USB 3.1 power channels

As previously stated, the power bus of the USB Type-C connector can handle up to 100 W (20 V / 5 A) when the cable is rated to such power. However, most applications will not use this high power capability. Therefore, the power bus filter must be designed to tolerate the power to be used by the application.

The USB 3.1 standard states a data rate of to 5 GBits/s (Gen 1) and 10 GBit/s (Gen 2). To attenuate any high frequency noise coupling to the power line, a low pass filter can be used with a cut-off frequency of approximately 1/10th of the data rate.

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5.2. 100 W (20 V / 5 A) applications

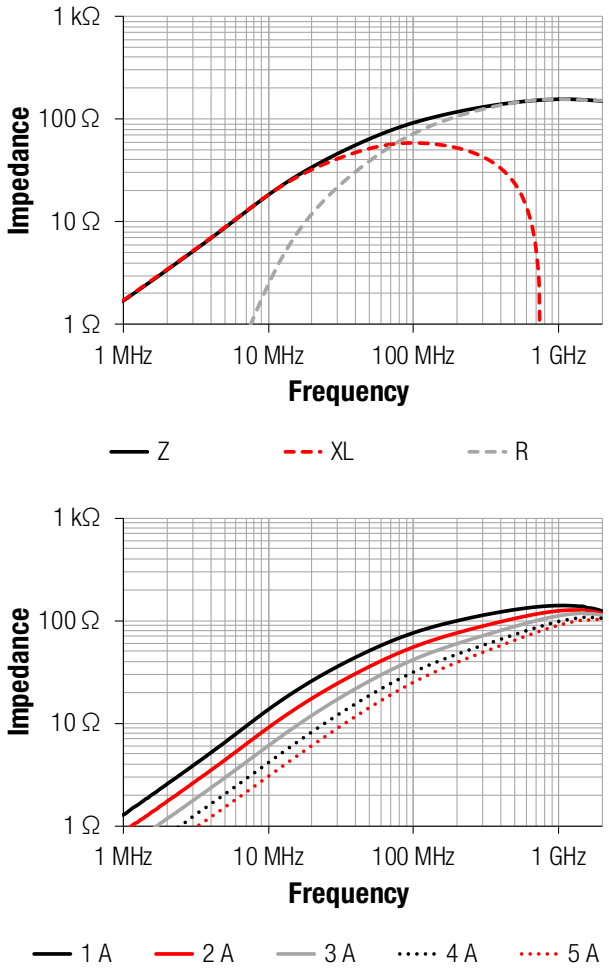

Figure 22: Complex impedance curve and the effect of DC current on the impedance of the WE-MPSB SMD ferrite (742 792 261 01)

The WE-MSPB (**742 792 261 01**) ferrite has its maximum impedance in the range from approximately 100 MHz to 1000 MHz in which the highest level of interference is to be anticipated in USB data transmission. At 750 MHz the ferrite acts like an ohmic resistor with no reactive components. Above this resonance frequency, the capacitive behavior dominates the impedance. Table 1 shows an overview of the most important parameters, the impedance curve is presented in Figure 22.

Properties	Test conditions	Value	Tolerance
Z	100 MHz	100 Ω	± 25 %
Z_{max}	1100 MHz	160 Ω	Typ.
I_R	ΔT = 40 K	8 A	Max.
R_{DC}		4.5 Ω	Max.

Table 1: Electrical data of WE-MPSB SMD ferrite (742 792 261 01)

Properties	Test conditions	Value	Tolerance
C	1±0.2 V_{RMS}; 1 kHz ± 10 %	4.7 µF	± 20 %
U_R		25 V	Max.
DF	1±0.2 V_{RMS}; 1 kHz ± 10 %	≤ 10 %	Typ.
R_{ISO}	Apply U_R for 120 s max	≥ 0.02 GΩ	

Table 2: WCAP-CSGP (885 012 107 018) electrical characteristics

Additionally, a filter is required to bypass any additional high frequency noise. A π-filter was chosen as they have a high insertion loss because both the source and the sink in the power supply are of low impedance. This gives rise to an optimal mismatch and therefore maximum suppression. The following filter was implemented using well-known filter equations.

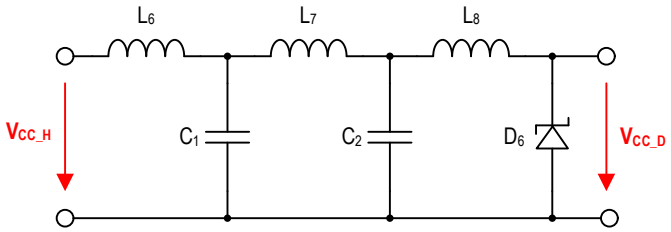

Figure 23: Implemented SMD ferrites, π-filter and TVS diode topology for 100 W power capability

Index	Serie	Order Code	Value
L_6	WE-MPSB 1812	**742 792 261 01**	100 Ω
L_7	WE-MAPI 4020	**744 383 560 12**	1.2 µH
L_8	WE-MPSB 1812	**742 792 261 01**	100 Ω
C_1	WCAP-CSGP 0805	**885 012 107 018**	4.7 µF / 25 V
C_2	WCAP-CSGP 0805	**885 012 107 018**	4.7 µF / 25 V
D_6	WE-TVS	**824 045 810**	20 V

Table 3: Selected components for the 100 W design

5.3. 60 W (20 V / 3 A) Applications

As a specialized cable is needed to handle 100 W of power, most applications will use 60 W or lower, which is the highest rated power of a 'normal' cable. Therefore, it may not be necessary to implement a filter that can handle 100 W. The following filter is implemented in a similar way to the 100 W filter but uses components with lower current handling capability and therefore, a more compact design.

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Index	Serie	Order Code	Value
L_6	WE-MPSB 1206	742 792 211 11	110 Ω
L_7	WE-MAPI 3020	744 383 360 12	1.2 µH
L_8	WE-MPSB 1812	742 792 261 01	100 Ω
C_1	WCAP-CSGP 0805	885 012 107 018	4.7 µF / 25 V
C_2	WCAP-CSGP 0805	885 012 107 018	4.7 µF / 25 V
D_6	WE-TVS	824 045 810	20 V

Table 4: Selected components for the 60 W design

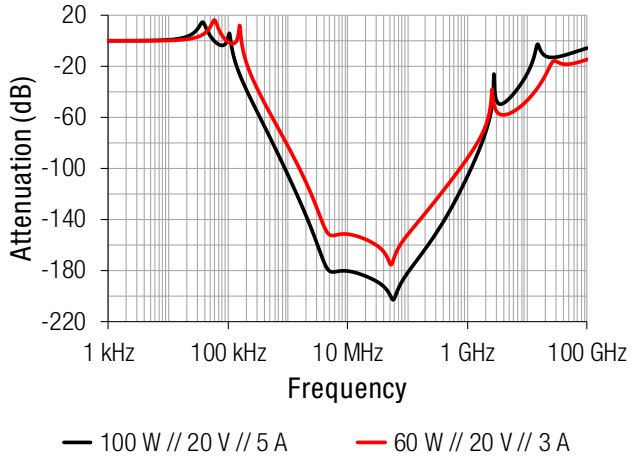

Figure 24: Simulated attenuation of the power line filter rated for 60 W and 100 W in comparison

5.4. USB 3.1 SuperSpeed+ channels

The WE-CNSW HF (744 233 56 00) is the heart of the data line filter. On account of its winding technology, the WE-CNSW HF has a high degree of symmetry and low parasitic capacitances. The structure is shown in Figure 25 and the most important parameters are given in Table 5

Properties	Test conditions	Value	Tolerance
Z	100 MHz	60 Ω	± 25 %
U_R		20 V	Typ.
I_R	ΔT = 20 K	600 mA	Max.
R_{DC}	T = 20 °C	220 mΩ	Max.

Table 5: Electrical characteristics of the current-compensated choke (744 233 56 00)

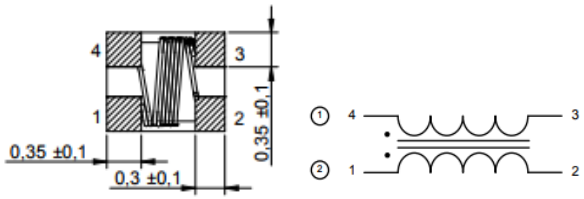

Figure 25: WE-CNSW HF (744 233 56 00) for the data line filter

The impedance curve and insertion loss of the CMC in common and differential mode is presented in Figure 26. Common mode noise occurs when the same interference components propagate in the same direction on the positive and negative channels with respect to ground. This is always the case for capacitive or inductive coupling on the circuit or its conductor tracks. Therefore, this impedance component must be as high as possible. At 100 MHz the CMC has around 60 Ω. The differential mode impedance occurs due to the stray inductance of the winding structure. This impedance must be as small as possible at the data frequency.

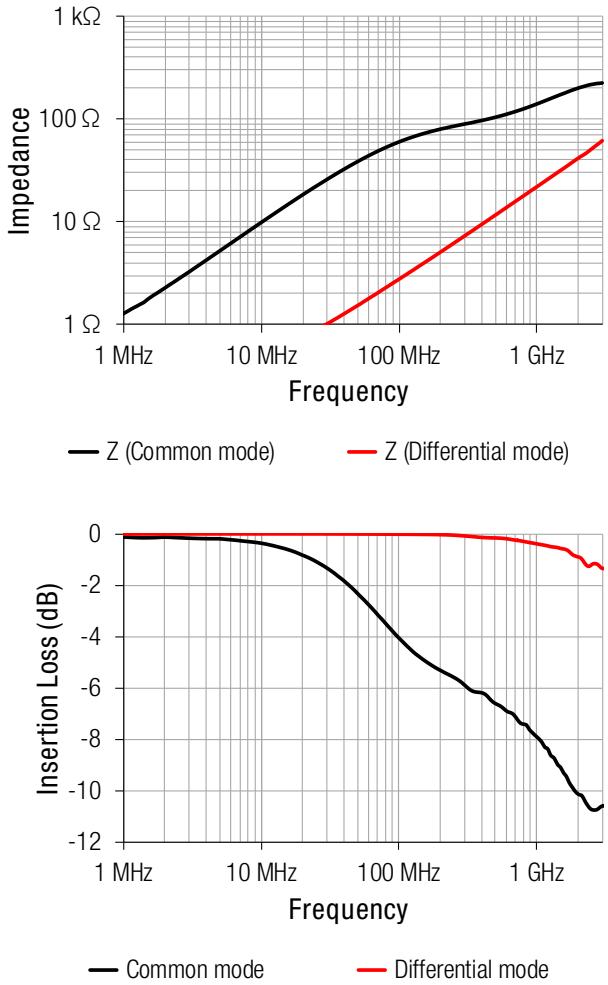

Figure 26: Impedance curve and insertion loss of WE-CNSW HF @ 50 Ω (744 233 56 00)

Including capacitance in the filter forms a low-pass second order filter. A diode array is used here instead of capacitors. The integrated diodes also have a parasitic capacitance, which can be effectively used. In addition, the parasitic inductance of the TVS diodes in the array is very low. This is necessary to attain a short response time to the overvoltage transients. Therefore, an almost ideal capacitor is combined with effective transient protection. The most important electrical

characteristics and the structure of the array are presented in Table 6 and Figure 27.

Properties	Test conditions	Value
C_{Ch}	V_{GND} = 0 V; $V_{I/O}$ = 1.65 V; f = 1 MHz; I/O to GND	0.18 $pF_{typ.}$ 0.27 $pF_{max.}$
C_X	V_{GND} = 0 V; $V_{I/O}$ = 1.65 V; f = 1 MHz; I/O to I/O	0.04 $pF_{typ.}$ 0.08 $pF_{max.}$

Table 6: Electrical characteristics of the WE-TVS Super Speed Series (824 012 823)

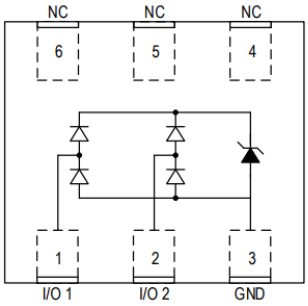

Figure 27: Electrical schematic and structure of the diode array WE-TVS (824 012 823)

5.5. Layout

The circuit board with its conductor tracks is an arrangement of components with capacitances and inductances. The layout therefore has to be designed according to the circuit requirements. A simple LC low-pass filter can be significantly impaired in its effectiveness by an unfavorable layout (Figure 28).

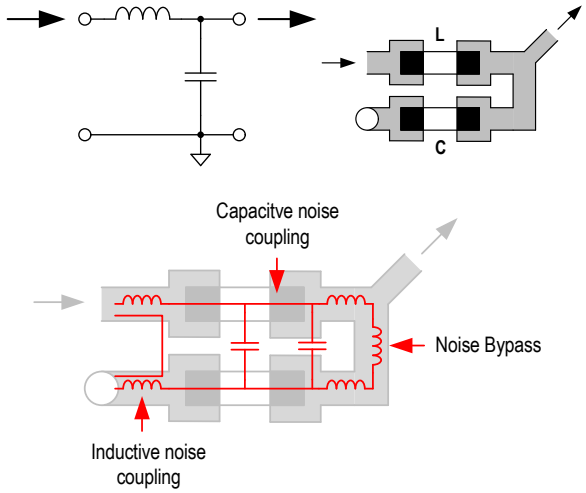

Figure 28: Example of a low-pass filter for high frequencies with an unfavorable layout

There are a number of issues with the above layout, which include:

- The ground connection to the capacitor is too long. 1 cm of track corresponds to 6-10 nH inductance.
- The ground connection should pass directly to the housing, as the ground reference of the cable shielding and the ground reference of the filter must lie on the same HF potential.
- A stub line to the capacitor passes between the inductor and capacitor. This stub line is an additional inductance in series with the capacitor and, as a result of the higher reactance of the inductance with increasing frequency, renders the capacitor ineffective.
- The filter input and filter output couple inductively with each other. The filter is short-circuited with increasing frequencies.
- The components couple capacitively as they are located parallel to one other. Here too, the coupling is greater with increasing frequency.

The corrected layout with the associated HF-compatible arrangement is shown in Figure 29.

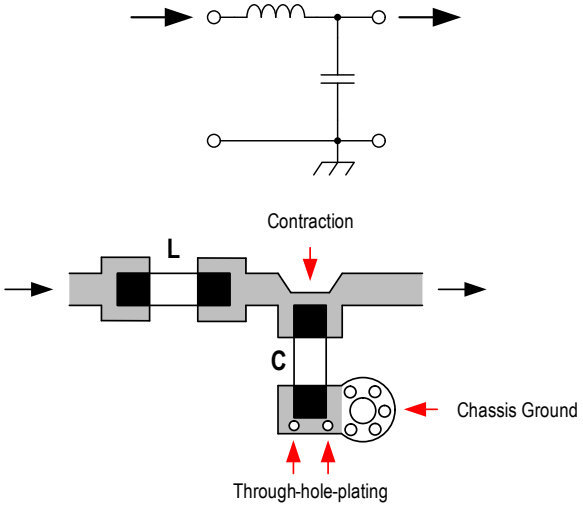

Figure 29: HF-optimized layout of an LC filter

This layout is better as:

- The contraction prevents interference current is bypassed at the capacitor. The capacitor "lies" in the signal path.
- The perpendicular arrangement of the components prevents mutual coupling.
- The short ground connection at the capacitor, which is of low impedance as a result of two through-contacts, offers an ideal high frequency reference point for the capacitor.

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5.6. Measurement

Measurement setup for measuring the connection quality with 1 m cable and associated eye diagram at 5 GBit/s (USB 3.1 Gen 1). The structure serves as the basis for subsequent measurements with the Type C dongle. Figure 32 shows the differential impedance Z_{diff} in a time domain representation, which corresponds to a distance from the reference plane on the left side (male connector). As components are added to the PCB, the effect on the signal can be observed. The first measurement was conducted with an unpopulated PCB. The second includes the CMC, the third the TVS diodes and the last shows the effect when the solder mask is applied. The basis is the adapter with all components and solder resist included. The receiver can open the eye again with the USB equalizer settings based upon the USB 3.1 r1.0 specification. With optimized components, you can achieve better results in advance and thus increase the range. The eye pattern test shows that the **WE-TVS** and **WE-CNSW HF** do not disturb the USB 3.1 signal. To refresh the signal, there is an equalizer in each USB receiver, which is responsible for opening the eye (Figure 30)

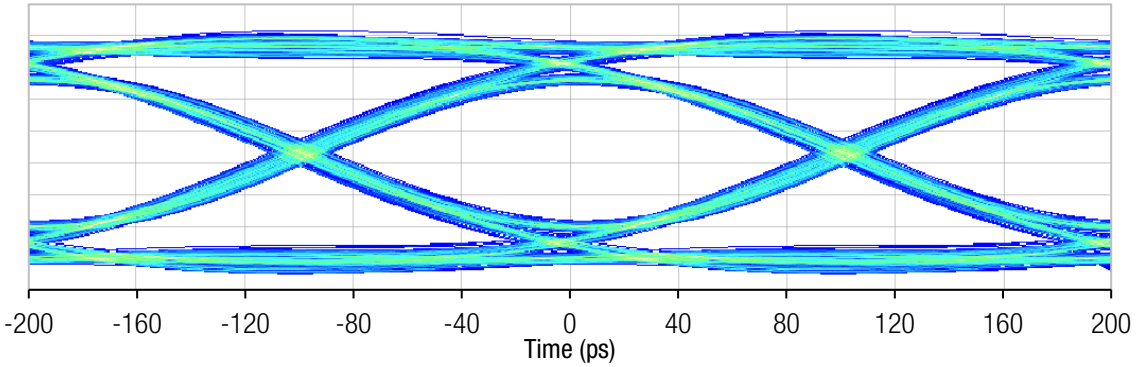

Figure 30: Eye diagram of the dongle with activated USB equalizer (@ 10 GBit/s)

6 Interface design kit

To facilitate the design of interfaces, Würth Elektronik has launched a dedicated Interface Design Kit (**744 999**). This design kit includes a design guide for USB 2.0 to USB 3.1, HDMI, CAN, Ethernet (100 and 1000 Base-T), VGA, DVI, RS232, RS485 interfaces and all the components used. These are ESD suppressors, SMD common mode chokes, chip bead ferrites, LAN transformers and the corresponding connectors. The color scheme makes it easy to locate the suitable parts for your application. Just follow the specific application color and select the suitable parts. For each application, there is a simple block schematic, which shows how to place the different components to get the best result.

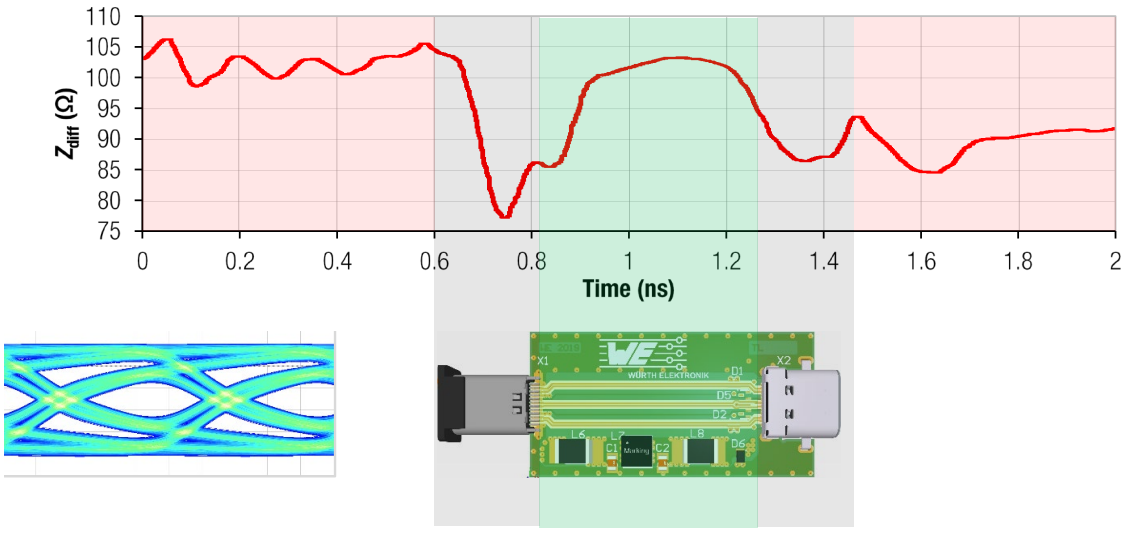

Figure 31: Time domain measurements and eye diagram of USB Type-C dongle

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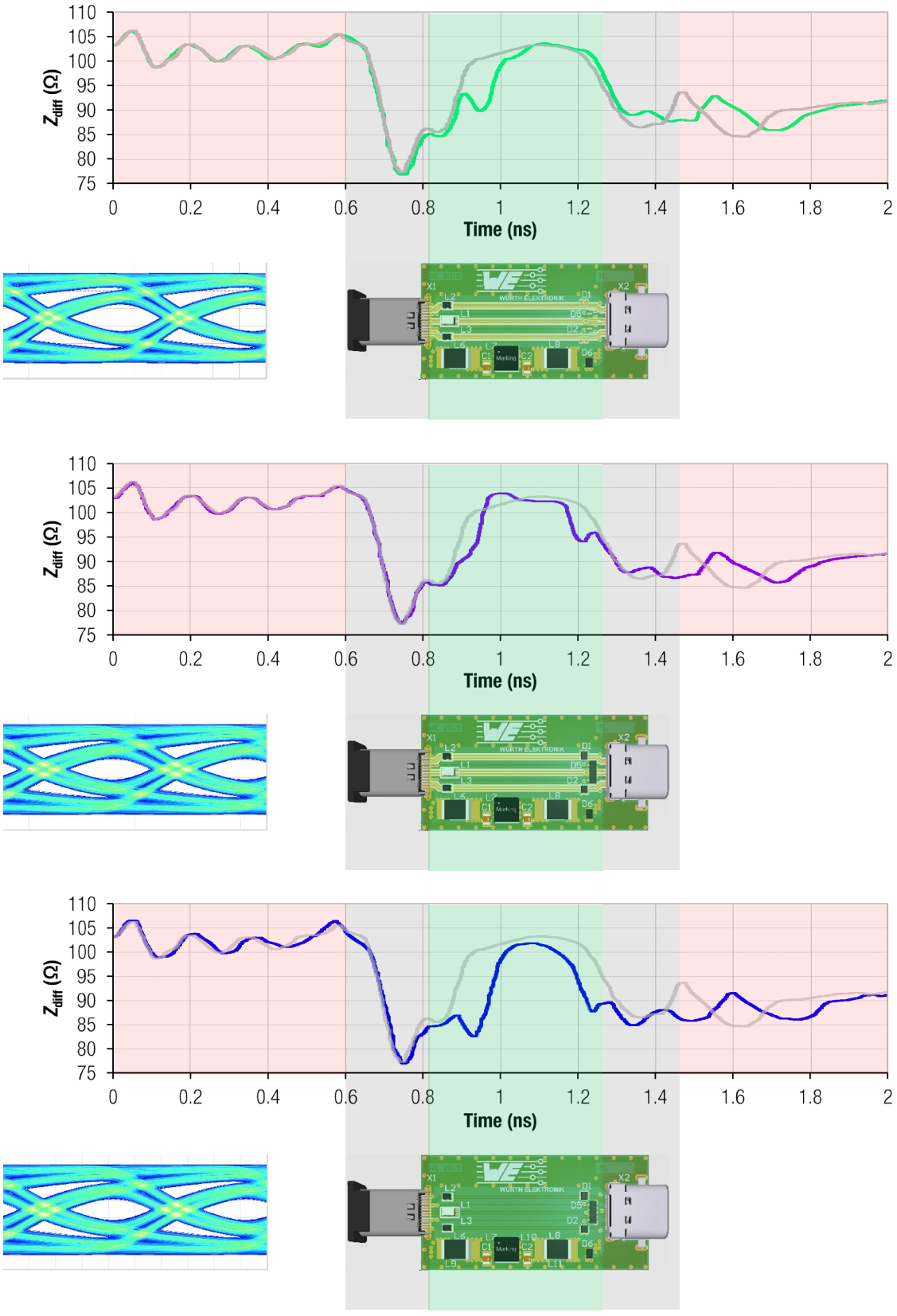

Figure 32: Time domain measurements and eye diagram of USB Type-C dongle

Application Note

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A. Appendix

A.1. Bill of Material (BOM)

Index	Description	Value	Size	Order Code
C_1 / C_2	WCAP-CSGP Ceramic Capacitor, X5R	C = 4.7 µF (25 V)	0805	885 012 107 018
D_1 / D_2 / D_3 / D_4	WE-TVS Super Speed TVS Diode Array, 2 channel ESD Protection,	V_{DC} = 3,3 V; I_{Peak} = 3 A; $V_{ESD,Contact/Air}$ = 8/15 kV	DFN1210-6L	824 012 823
D_5	WE-TVS Super Speed TVS Diode Array, 8 channel ESD Protection	V_{DC} = 5 V; I_{Peak} = 5 A; $V_{ESD,Contact/Air}$ = 15/15 kV	DFN3810-9L	824 014 885
D_6	WE-TVS Standard Speed TVS Diode, Unidir, ESD Protection	V_{DC} = 20 V; I_{Peak} = 24 A; $V_{ESD,Contact/Air}$ = 30/30 kV	DFN1610-2L	824 045 810
L_1	WE-CNSW Common Mode Choke,	L = 90 Ω @ 100 MHz	0805	744 231 091
L_2 / L_3 / L_3 / L_4	WE-CNSW HF Common Mode Choke	L = 60 Ω @ 100 MHz	0504	744 233 56 00
L_6 / L_8	WE-MPSB Multilayer Power Suppression Bead,	L = 100 Ω @ 100 MHz, I_R = 8 A, ESR = 6 mΩ	1812	742 792 261 01
L_7	WE-MAPI SMT Inductor	L = 1.2 µH, I_R = 5.8 A	4020	744 383 560 12
R_1 / R_2	Resistor	R = 2.2 kΩ	1206	Generic
X_1	WR-COM; Male USB 3.1 Type C 24 pins 90° THT & SMT LP 0.8			632 712 000 011
X_2	WR-COM Female USB 3.1 Type C 24 pins 90° THT & SMT LP 1.0			632 723 130 112

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CONTACT INFORMATION

appnotes@we-online.com
Tel. +49 7942 945 - 0

Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Str. 1 · 74638 Waldenburg · Germany
www.we-online.com