2 Channel I²C Isolator

DESCRIPTION

The CDI2C 18032x11 is a bidirectional channel isolator series compatible with I²C bus interface that provides capacitive isolation between the primary and secondary sides of the device.

The 18032x11 offers two open-drain channels. The 18032011 provides bidirectional serial data (SDA) and serial clock (SCL) pins. The 18032111 contains bidirectional serial data (SDA) and unidirectional clock (SCL) pins.

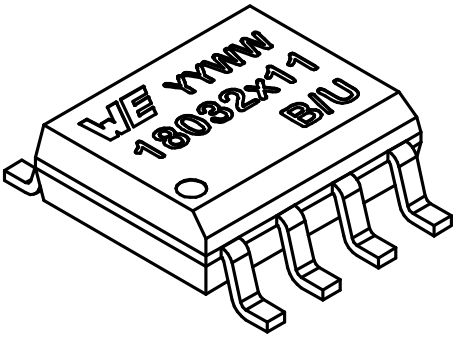
The 18032x11 isolators support bidirectional data transfer rates of up to 2.0 MHz, making them suitable for most I²C communication applications.

The I²C isolator requires two supply voltages, one for the side 1 and one for the side 2. The CDI2C ensures fast time to market and low development costs.

The I²C isolator is available in an SOIC-8NB package (4.9 x 6.0 x 1.8)mm.

FEATURES

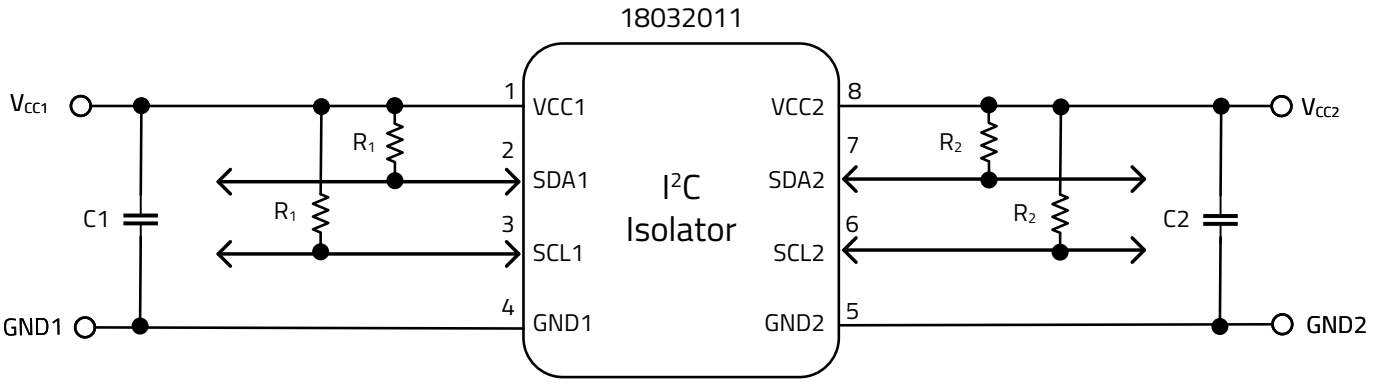
- Isolation Voltage: 3.75kV$_{RMS}$ for 60s
- Basic isolation
- Input voltage range: 3V to 5.5V
- Bidirectional data rate up to 2MHz
- ±150kV/µs typ. CMTI
- Open-drain output current-sink capability:
  - 3.5mA (Side 1)
  - 35mA (Side 2)
- Maximum allowed capacitive loading:
  - 40 pF (Side 1)
  - 400 pF (Side 2)
- Ambient temperature range: -40°C to 125°C
- RoHS and REACH compliant
- UL1577 recognized
- DIN EN IEC 60747-17 (VDE 0884-17): certified



TYPICAL APPLICATIONS

- Isolated I²C buses
- Battery management systems
- Motor control systems
- Isolated ADCs and DACs
- Isolated sensor interfaces

TYPICAL CIRCUIT DIAGRAM



The above diagram indicates only one of the possible channel configurations available.

CONTENTS

1 PINOUT

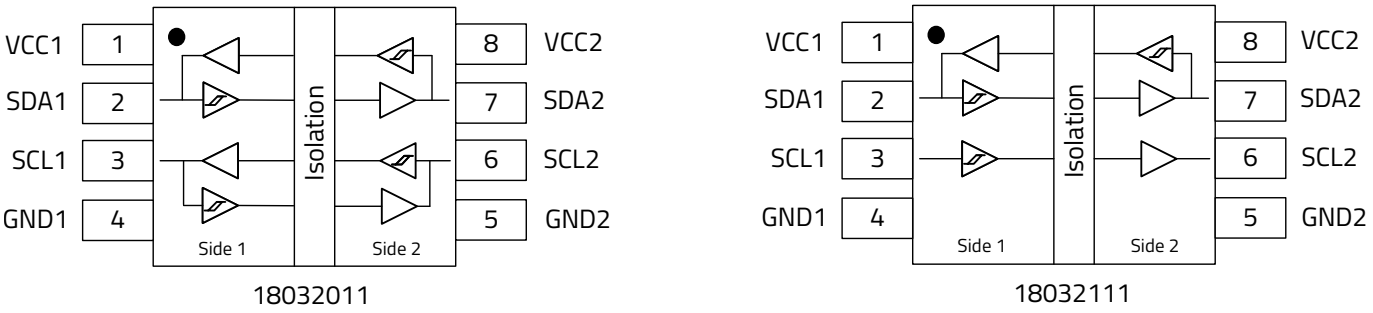


Figure 1: Pinout.

Table 1: Marking description.

MARKING	DESCRIPTION
WE	Würth Elektronik eiSos GmbH & Co. KG
YYWW	Year and calendar week
18032x11	Order code
B/U	Number of bidirectional and unidirectional channels

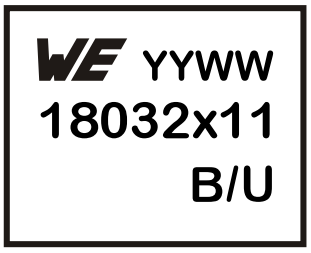


Figure 2: Marking.

Table 2: Pin description.

SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC1	1	Power	Supply input for side 1.
SDA1	2	I/O	Serial data input / output for side 1.
SCL1	3	I/O	Serial clock input / output for side 1.
GND1	4	Power	Ground for side 1.
GND2	5	Power	Ground for side 2.
SCL2	6	I/O	Serial clock input / output for side 2.
SDA2	7	I/O	Serial data input / output for side 2.
VCC2	8	Power	Supply input for side 2.

2 ORDERING INFORMATION

Table 3: Ordering information.

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
18032011	2 bidirectional channels	SOIC-8NB	13" Reel (2500 pieces)
18032111	1 bidirectional and 1 unidirectional channel		

3 SALES INFORMATION

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC and Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/digitalisolators Technical support: wpme-support@we-online.com

4 ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

SYMBOL	PARAMETER	LIMIT		UNIT
		MIN[1]	MAX[1]	
VCC1, VCC2	Supply voltage pins	-0.5	6	V
V_{SDAX}, V_{SCLX}	Voltage at SDA1, SCL1, SDA2 and SCL2 pins	-0.5	V_{CCX} + 0.5[2]	V
I_{OUT_X1}	SDA1 / SCL1 channel output current	-20	20	mA
I_{OUT_X2}	SDA2 / SCL2 channel output current	-100	100	mA
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
V_{ESD}	ESD voltage (HBM), all pins[4]	-8	8	kV
V_{ESD}	ESD voltage (CDM), all pins[4]	-2	2	kV

5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are either referenced to GND1 or GND2.

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C.

Table 5: Operating conditions.

SYMBOL	PARAMETER	MIN[1]	TYP[3]	MAX[1]	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3	—	5.5	V
V_{SDA1}, V_{SCL1}	Input / Output signal voltages for side 1	0	—	V_{CC1}	V
V_{SDA2}, V_{SCL2}	Input / Output signal voltages for side 2	0	—	V_{CC2}	V
V_{IH1}	Logic high input threshold for side 1	0.7×V_{CC1}	—	V_{CC1}	V
V_{IL1}	Logic low input threshold for side 1	0	—	0.47	V
V_{IH2}	Logic high input threshold for side 2	2	—	V_{CC2}	V
V_{IL2}	Logic low input threshold for side 2	0	—	0.8	V
I_{OL1}	Logic low output sink current for side 1	0.5	—	3.5	mA
I_{OL2}	Logic low output sink current for side 2	0.5	—	35	mA
C_1	Maximum capacitive load for side 1	—	—	40	pF
C_2	Maximum capacitive load for side 2	—	—	400	pF
f_{max}	Maximum Clock Frequency[7]	—	2	—	MHz
T_a	Ambient temperature range	-40	—	125	°C

6 ELECTRICAL SPECIFICATIONS

Caution:
MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C. Typical values represent statistically the utmost probable values at T_A = 25°C, unless otherwise noted.

Table 6: Electrical specifications part 1.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(3)	MAX(1)	UNIT
Supply Characteristics						
V_{CCX_UVLO}	Supply undervoltage-lockout threshold(9)		1.95	2.24	2.53	V
Channel Characteristics						
For Side 1						
V_{IHT1}	High-level logic input threshold (SDA1 and SCL1)		500	560	620	mV
V_{ILT1}	Low-level logic input threshold (SDA1 and SCL1)		470	500	520	mV
V_{HSY1}	Input voltage hysteresis	V_{IHT1} - V_{ILT1}	40	60	80	mV
V_{OL1}	Low-level output voltage (SDA1 and SCL1)(5)	0.5mA $\leq I_{SDA1}$ and $I_{SCL1} \leq$3.5mA	630	700	760	mV
ΔV_{OIT1}	Low-level output voltage to high-level output voltage threshold difference (SDA1 and SCL1)(5)(8)	0.5mA $\leq I_{SDA1}$ and $I_{SCL1} \leq$3.5mA	100	—	—	mV
For Side 2						
V_{IHT2}	High-level logic input threshold (SDA2 and SCL2)		1.55	1.75	1.97	V
V_{ILT2}	Low-level logic input threshold (SDA2 and SCL2)		1.13	1.33	1.53	V
V_{HSY2}	Input voltage hysteresis	V_{IHT2} - V_{ILT2}	0.30	0.42	0.54	V
V_{OL2}	Low-level output voltage (SDA2 and SCL2)	0.5mA $\leq I_{SDA2}$ and $I_{SCL2} \leq$35mA	—	—	0.4	V
For Both Sides						
I_L	Input leakage current, SDA1, SCL1, SDA2, SCL2	V_{SDAx} = V_{SCLx} = V_{CCx}	—	—	1	µA
C_{IN}	Input capacitance to respective ground		—	3	—	pF
CMTI	Common-mode transient immunity	Figure 12	—	150	—	kV/µs

Parameters indicated in electrical specifications part 1 are applicable across all part numbers with all input/output conditions unless otherwise specified.

Table 7: Electrical specifications part 2.

SYMBOL	PARAMETER	TEST CONDITIONS	DEFINITIONS	MIN [1]	TYP [3]	MAX [1]	UNIT
Timing Characteristics							
4.5V ≤V_{CC1} and V_{CC2} ≤5.5V							
t_{f1}	Output signal fall time (SDA1 and SCL1)	R_1 = 1.43kΩ C_1 = 40pF Figure 10	Side 1 input from $0.7 \times V_{CC1}$ to 0.3 ×V_{CC1}	—	11	14	ns
			Side 1 input from 0.9 ×V_{CC1} to 900mV	—	32	60	
t_{f2}	Output signal fall time (SDA2 and SCL2)	R_2 = 143Ω C_2 = 400pF Figure 10	Side 2 input from 0.7 ×V_{CC2} to 0.3 ×V_{CC2}	—	10	12	ns
			Side 2 input from 0.9 ×V_{CC2} to 400mV	—	22	36	
$t_{Loop121}$	Loop propagation delay on side 1[5]	R_1 = 1.43kΩ C_1 = 40pF R_2 = 143 Ω C_2 = 400pF Figure 11	0.4V to 0.3 ×V_{CC1}	—	150	230	ns
t_{PLH12}	Propagation delay, side 1 to side 2	R_1 = 1.43kΩ C_1 = 10pF R_2 = 143Ω C_2 = 10pF Figure 10	0.55V side 1 input to 0.7 ×V_{CC2} side 2 output	—	79	120	ns
t_{PHL12}	Propagation delay, side 1 to side 2		0.7V side 1 input to 0.4V side 2 output	—	79	90	ns
PWD_{12}	Pulse width distortion, side 1 to side 2		$\lvert t_{PHL12} - t_{PLH12} \rvert$	—	30	—	ns
t_{PLH21}	Propagation delay, side 2 to side 1[5]		0.4 ×V_{CC2} side 2 input to 0.7 ×V_{CC1} side 1 output	—	64	130	ns
t_{PHL21}	Propagation delay, side 2 to side 1[5]		0.4 ×V_{CC2} side 2 input to 0.9V side 1 output	—	74	150	ns
PWD_{21}	Pulse width distortion, side 2 to side 1[5]		$\lvert t_{PHL21} - t_{PLH21} \rvert$	—	12	—	ns

Table 8: Electrical specifications part 3.

SYMBOL	PARAMETER	TEST CONDITIONS	DEFINITIONS	MIN [1]	TYP [3]	MAX [1]	UNIT
Timing Characteristics							
3V ≤V_{CC1} and V_{CC2} ≤3.6V							
t_{f1}	Output signal fall time (SDA1 and SCL1)	R_1 = 953Ω C_1 = 40pF Figure 10	Side 1 input from 0.7 ×V_{CC1} to 0.3 ×V_{CC1}	—	19	28	ns
			Side 1 input from 0.9 ×V_{CC1} to 900mV	—	31	48	
t_{f2}	Output signal fall time (SDA2 and SCL2)	R_2 = 95.3Ω C_2 = 400pF Figure 10	Side 2 input from 0.7 ×V_{CC2} to 0.3 ×V_{CC2}	—	13	20	ns
			Side 2 input from 0.9 ×V_{CC2} to 400mV	—	28	60	
$t_{Loop121}$	Loop propagation delay on side 1[5]	R_1 = 953Ω C_1 = 40pF R_2 = 95.3 Ω C_2 = 400pF Figure 11	0.4V to 0.3 ×V_{CC1}	—	154	220	ns
t_{PLH12}	Propagation delay, side 1 to side 2	R_1 = 953Ω C_1 = 10pF R_2 = 95.3Ω C_2 = 10pF Figure 10	0.55V side 1 input to 0.7 ×V_{CC2} side 2 output	—	79	135	ns
t_{PHL12}	Propagation delay, side 1 to side 2		0.7V side 1 input to 0.4V side 2 output	—	91	130	ns
PWD_{12}	Pulse width distortion, side 1 to side 2		$\lvert t_{PHL12} - t_{PLH12} \rvert$	—	11	—	ns
t_{PLH21}	Propagation delay, side 2 to side 1[5]		0.4 ×V_{CC2} side 2 input to 0.7 ×V_{CC1} side 1 output	—	52	100	ns
t_{PHL21}	Propagation delay, side 2 to side 1[5]		0.4 ×V_{CC2} side 2 input to 0.9V side 1 output	—	81	120	ns
PWD_{21}	Pulse width distortion, side 2 to side 1[5]		$\lvert t_{PHL21} - t_{PLH21} \rvert$	—	29	—	ns

Table 9: Electrical specifications part 4.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18032011 4.5V ≤V_{CC1} and V_{CC2} ≤5.5V						
I_{CC1}	Primary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	5.0	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 and C_2 = OPEN	—	2.4	–	mA
I_{CC2}	Secondary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	4.7	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	2.2	–	mA
18032111 4.5V ≤V_{CC1} and V_{CC2} ≤5.5V						
I_{CC1}	Primary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	3.0	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	1.8	–	mA
I_{CC2}	Secondary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	2.5	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	1.9	–	mA
18032011 3V ≤V_{CC1} and V_{CC2} ≤3.6V						
I_{CC1}	Primary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	4.9	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	2.4	–	mA
I_{CC2}	Secondary side external power supply input current	V_{SDA1} = V_{SCL1} = GND1; V_{SDA2} = V_{SCL2} = GND2; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	4.7	–	mA
		V_{SDA1} = V_{SCL1} = V_{CC1}; V_{SDA2} = V_{SCL2} = V_{CC2}; R_1 = R_2 = OPEN; C_1 = C_2 = OPEN	—	2.2	–	mA

Table 10: Electrical specifications part 5.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18032111 3.0V $\leq V_{CC1}$ and $V_{CC2} \leq$3.6V						
I_{CC1}	Primary side external power supply input current	$V_{SDA1} = V_{SCL1}$ = GND1; $V_{SDA2} = V_{SCL2}$ = GND2; $R_1 = R_2$ = OPEN; $C_1 = C_2$ = OPEN	—	2.9	–	mA
		$V_{SDA1} = V_{SCL1} = V_{CC1}$; $V_{SDA2} = V_{SCL2} = V_{CC2}$; $R_1 = R_2$ = OPEN; $C_1 = C_2$ = OPEN	—	1.7	–	mA
I_{CC2}	Secondary side external power supply input current	$V_{SDA1} = V_{SCL1}$ = GND1; $V_{SDA2} = V_{SCL2}$ = GND2; $R_1 = R_2$ = OPEN; C_1 and C_2 = OPEN	—	2.4	–	mA
		$V_{SDA1} = V_{SCL1} = V_{CC1}$; $V_{SDA2} = V_{SCL2} = V_{CC2}$; $R_1 = R_2$ = OPEN; $C_1 = C_2$ = OPEN	—	1.8	–	mA

7 ISOLATION SPECIFICATIONS

Table 11: Isolation specification table.

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR	External clearance	Shortest distance through air between terminals	4	mm
CPG	External creepage	Shortest distance across package surface between terminals	4	mm
DTI	Distance through the insulation	Minimum internal clearance	28	µm
C_{IO}	Barrier capacitance, input to output	V_{IO} = 0.4 x sin (2πft), f = 1MHz	1	pF
R_{IO}	Isolation resistance	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C≤T_A ≤ 125°C	>10^{11}	Ω
		V_{IO} = 500V at T_A = 150°C	>10^{9}	Ω
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	IEC 60664-1 Material group		I	
	IEC 60664-1 overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-IV	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10				
V_{IORM}	Max. repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Max. working isolation voltage	AC voltage; Time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Max. transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1s (100% production)	5300	V_{PK}
V_{IMP}	Max. impulse voltage	Test method per IEC 62368-1, 1.2/50 µs waveform	5000	V_{PK}
V_{IOSM}	Max. surge isolation voltage	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.3 x V_{IMP} (qualification)	6500	V_{PK}
q_{pd}	Apparent charge	Method a, after input/output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10s	≤5	pC
		Method b, at routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s	≤5	pC
	Pollution degree		2	
UL1577				
$V_{ISO(max)}$	Max. withstanding isolation voltage(6)	V_{TEST} = V_{ISO}, t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO}, t = 1s (100% production)	3750	V_{RMS}

8 APPROVALS

Table 12: Approvals.

STANDARD	DESCRIPTION
UL 1577	UL File No: E535458
DIN EN IEC 60747-17 (VDE 0884-17):2021-10	40058073

9 RoHS, REACH

Table 13: RoHS, REACH.

RoHS directive	COMPLIANT RoHS&REACH WÜRTH ELEKTRONIK	Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACH directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH).

10 PACKAGE SPECIFICATIONS

Table 14: Package specifications.

ITEM	PARAMETER	TYP[3]	UNIT
Lead finish	Matte Sn	—	—
Weight	—	0.075	g

11 NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) This value must never exceed 6V.

(3) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(4) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114. The charged device model test method is per JESD22-C101.

(5) This parameter is only valid for bidirectional channels of 18032011 and 18032111.

(6) 100% final production tested value. The qualified isolation voltage value is 3.75kV$_{RMS}$. For detailed isolation characteristics see the isolation specification table (Isolation specification table).

(7) The maximum operating frequency is specified for the maximum supported bus capacitance and output current. Higher operating frequencies may be achievable with reduced bus capacitance.

(8) $\Delta V_{OIT1} = V_{OL1} - V_{IHT1}$, is the minimum voltage margin between logic low output and logic high input to prevent bidirectional I²C bus latch.

(9) The device enters lockout if either side's supply voltage falls below the minimum level and operates normally only when both sides' supply voltage levels exceed the release threshold.

12 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: T_A = 25°C.

12.1 DC Performance Curves

The curves shown below use the test conditions indicated in the corresponding parameter described in the ELECTRICAL SPECIFICATIONS.

12.1.1 Output Fall Time vs. Ambient Temperature

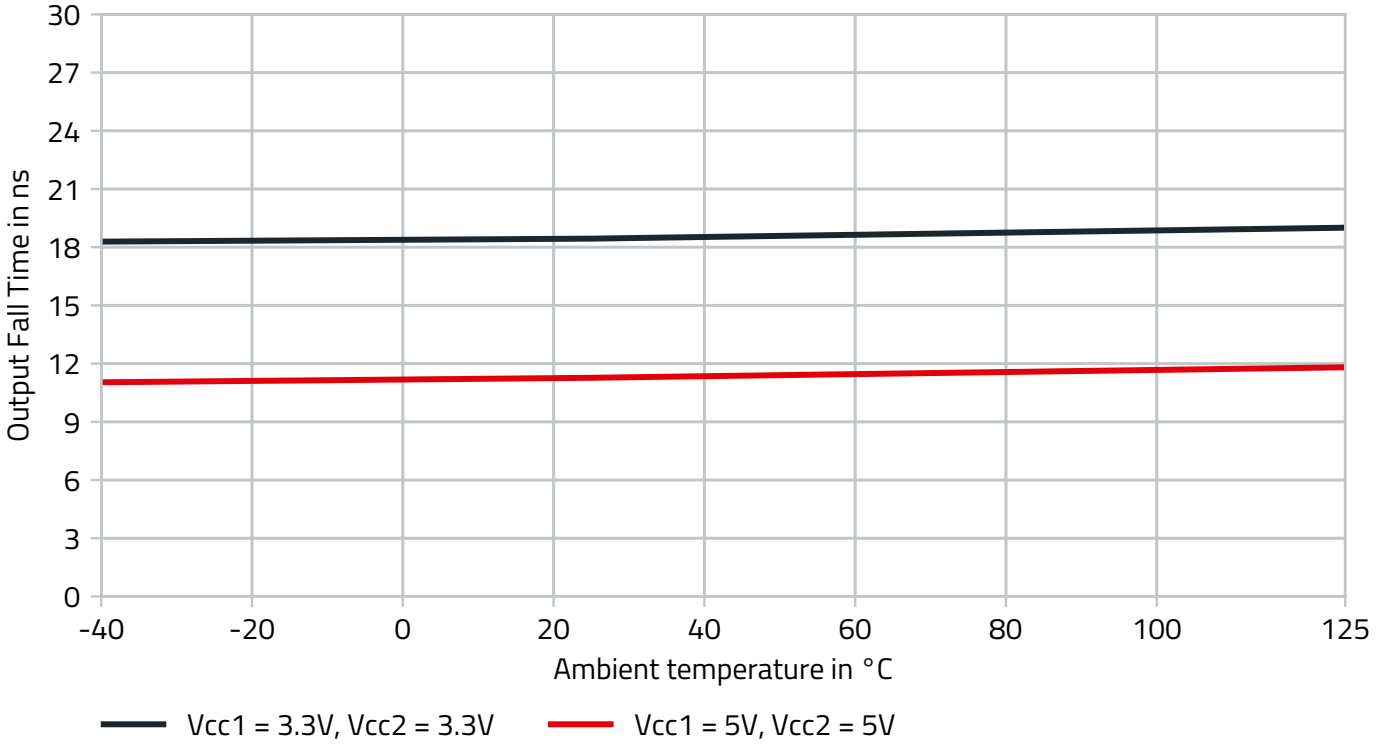


Figure 3: 18032x11 output fall time for side 1

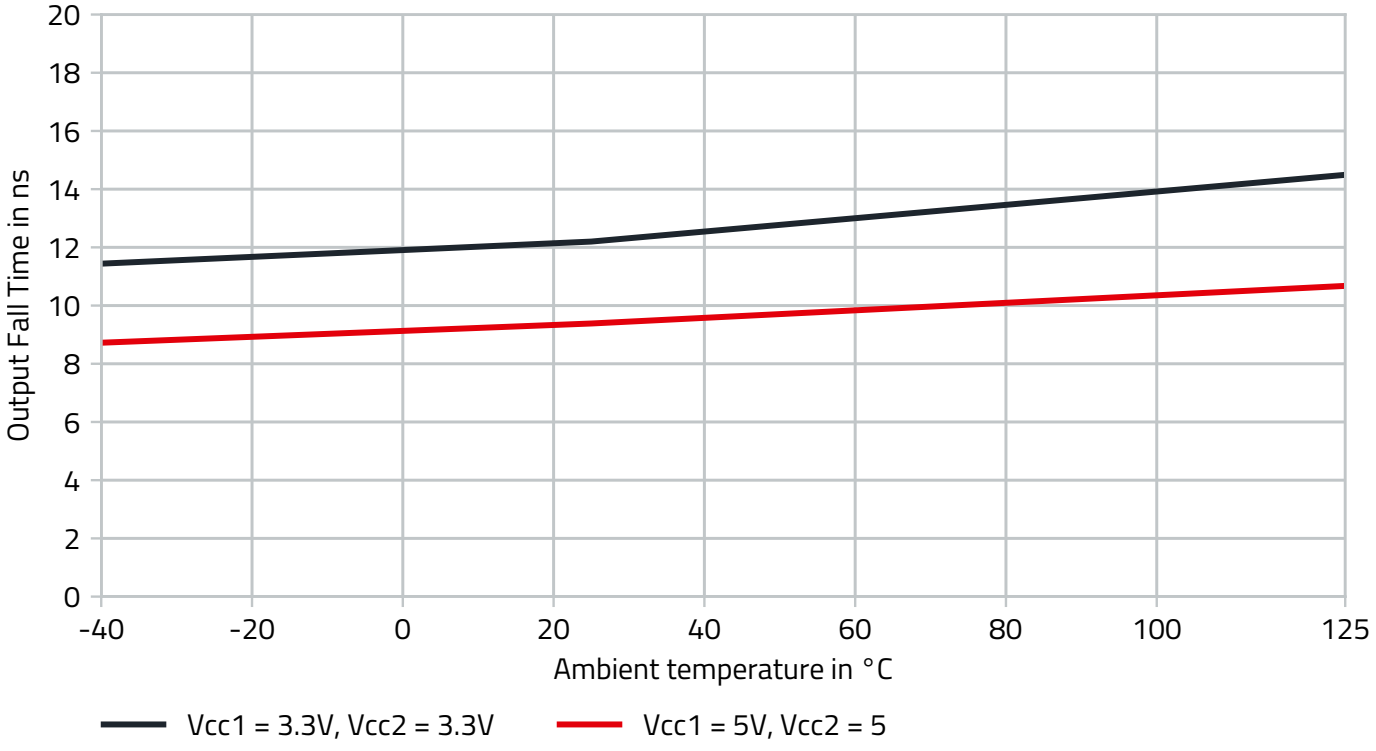


Figure 4: 18032x11 output fall time for side 2

12.1.2 Propagation Delay from Side 1 to 2 vs. Ambient Temperature

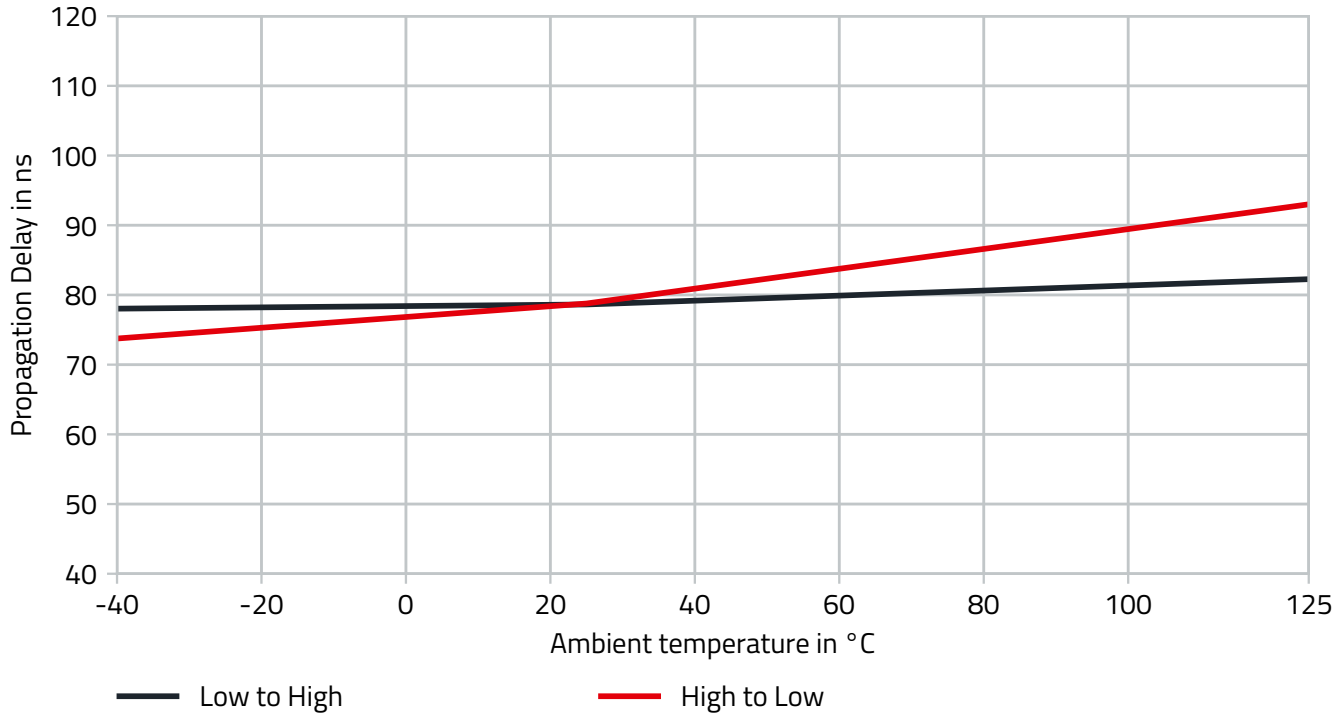


Figure 5: 18032x11 propagation delay from side 1 to 2 at V_{CC1} = 5V, V_{CC2} = 5V

12.1.3 Propagation Delay from Side 2 to 1 vs. Ambient Temperature

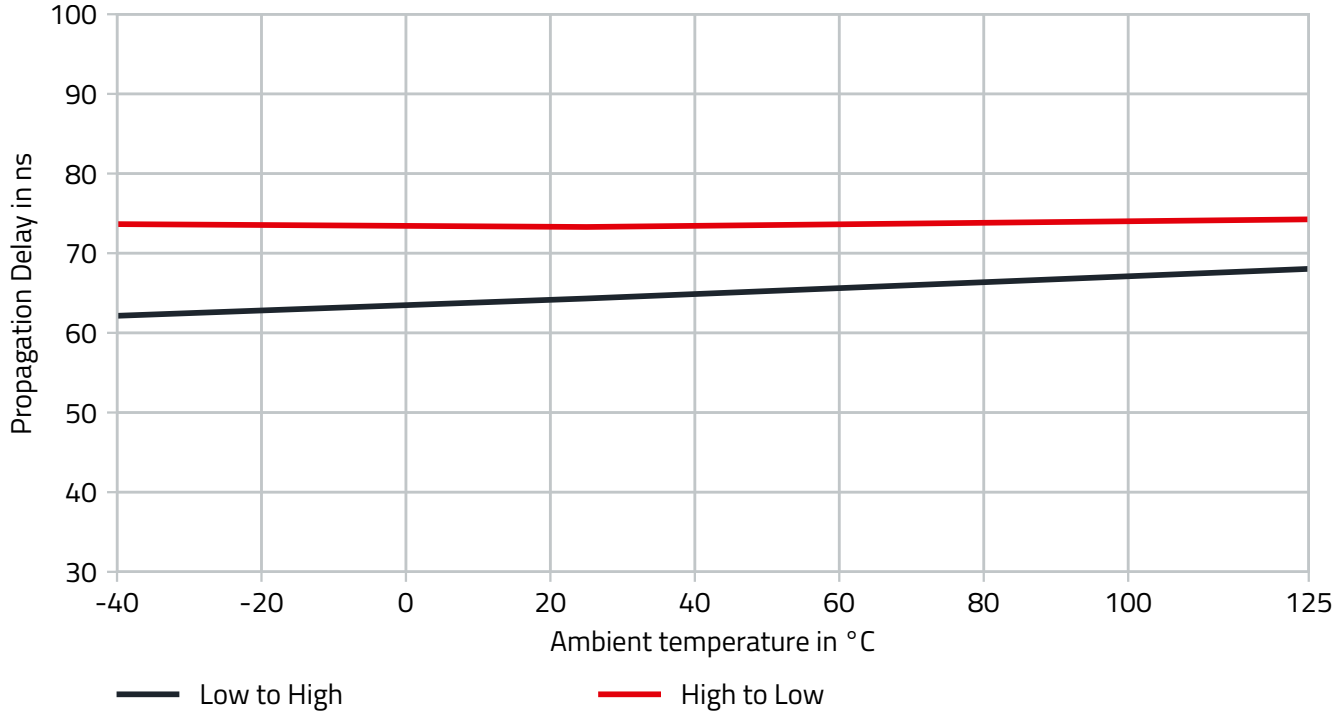


Figure 6: 18032x11 propagation delay high to low, from side 2 to 1 V_{CC1} = 5V, V_{CC2} = 5V

12.1.4 Loop Propagation Delay on Side 1 vs. Ambient Temperature

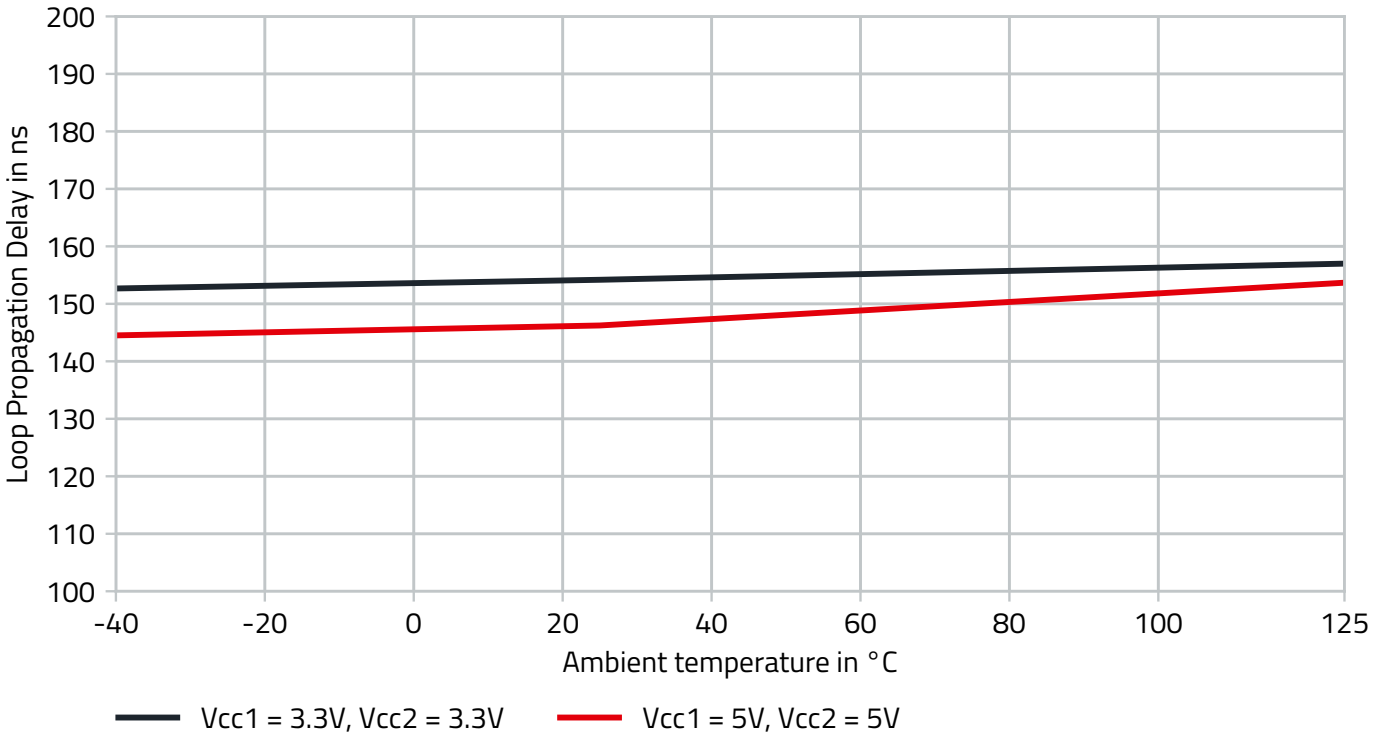


Figure 7: 18032x11[5] loop propagation delay on side 1

12.1.5 Safety Limiting Curves

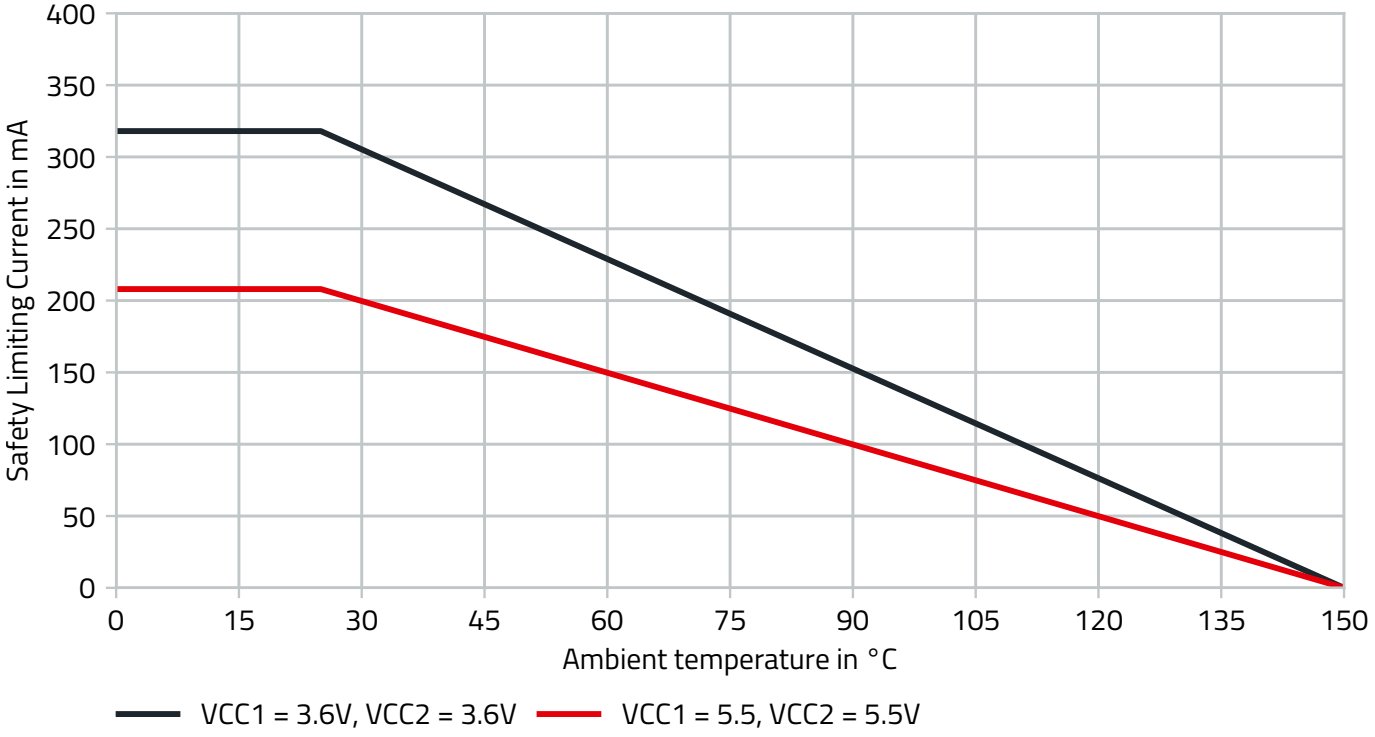


Figure 8: 18032x11 safety limiting current.

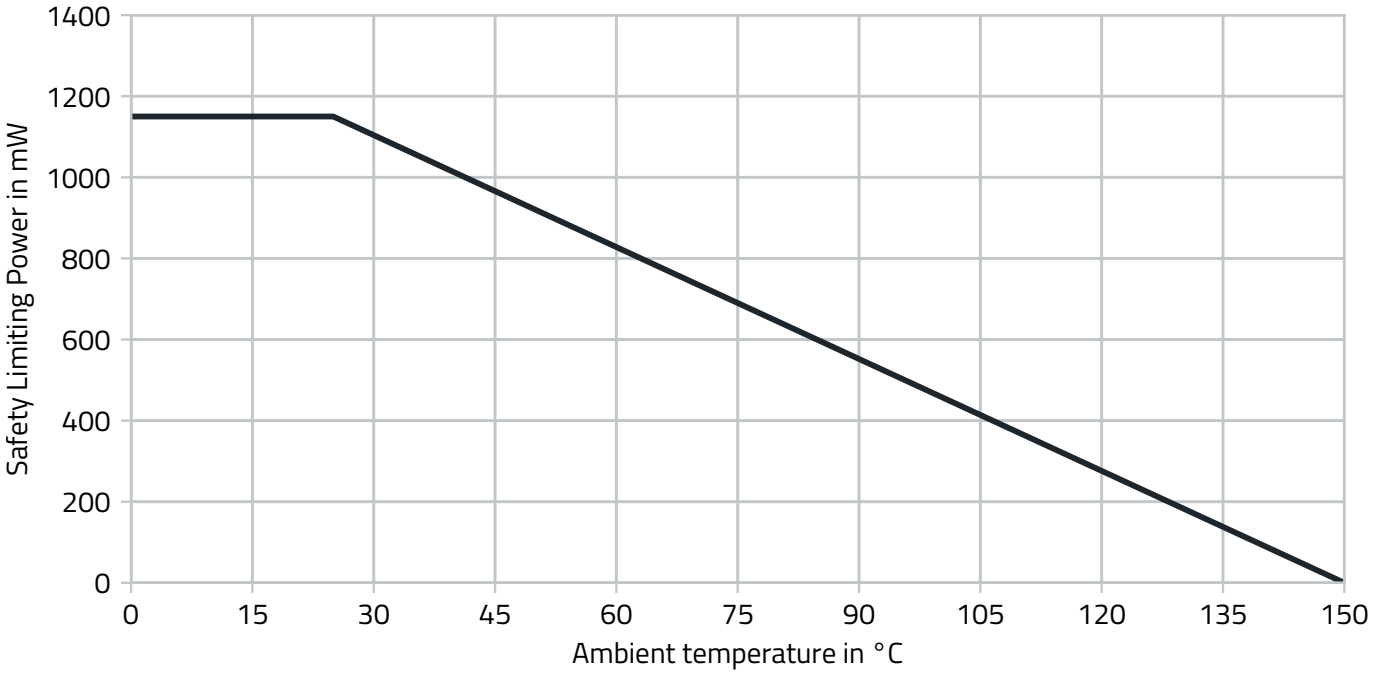


Figure 9: 18032x11 safety limiting power.

13 TRUTH TABLE

Table 15: I/O truth table.

POWER STATE	INPUT	OUTPUT
V_{CC1} or V_{CC2} < 1.95V	Undetermined	High impedance
V_{CC1} and V_{CC2} > 2.53V	Low level	Low level
V_{CC1} and V_{CC2} > 2.53V	High level	High impedance
V_{CC1} and V_{CC2} > 2.53V	High impedance	Undetermined

14 TEST SCHEMATICS

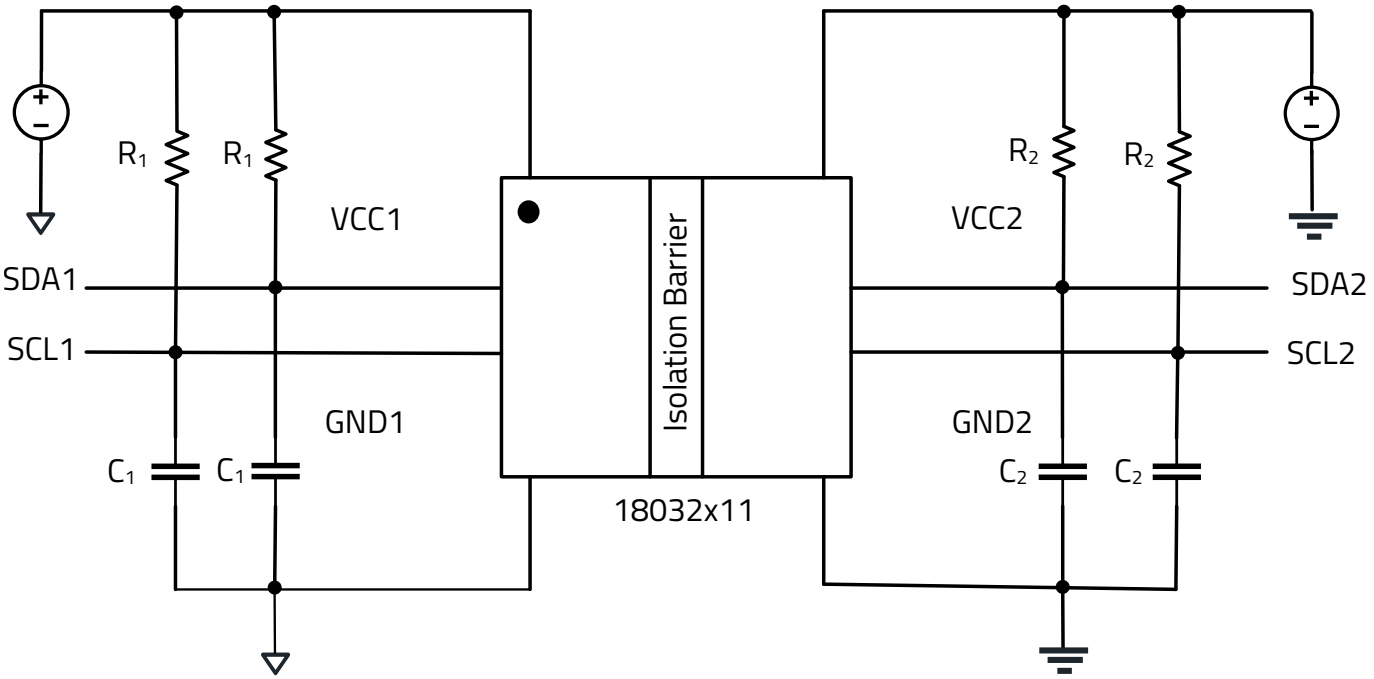


Figure 10: Fall time and propagation delay test schematic.

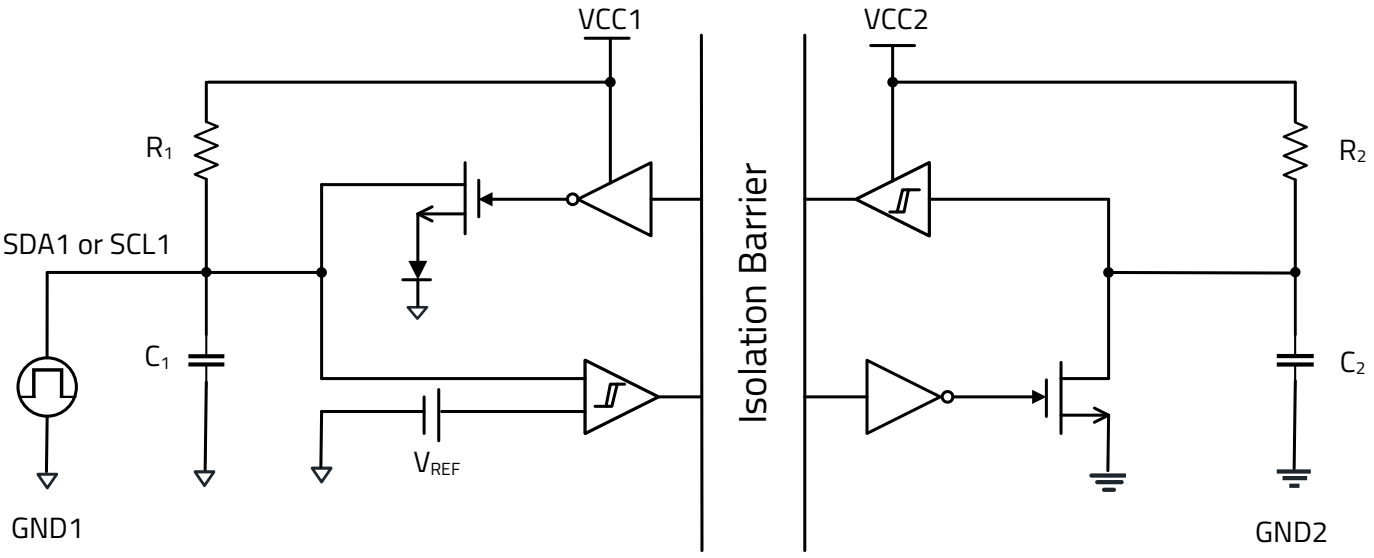


Figure 11: Loop propagation delay test schematic

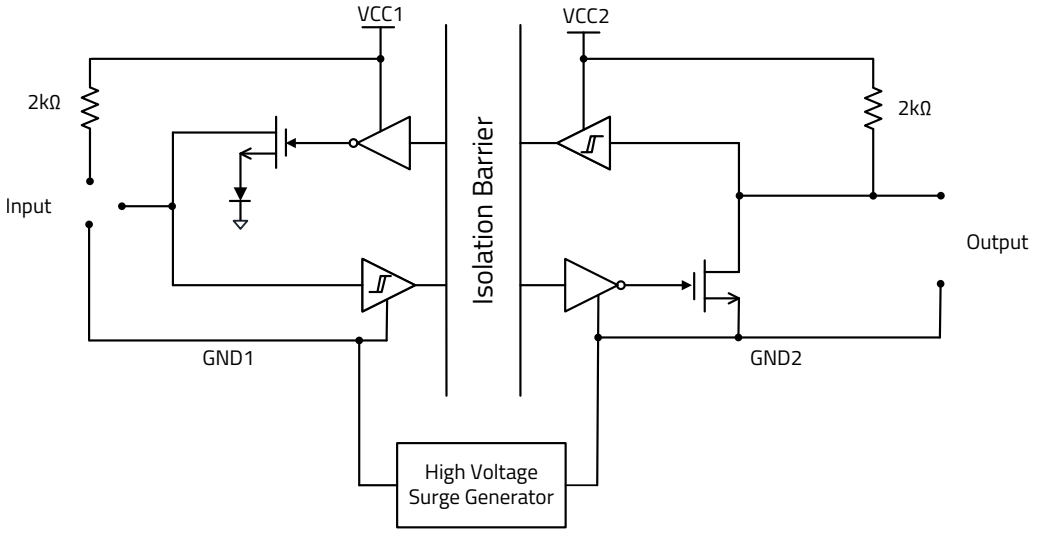


Figure 12: CMTI test schematic.

15 BLOCK DIAGRAM

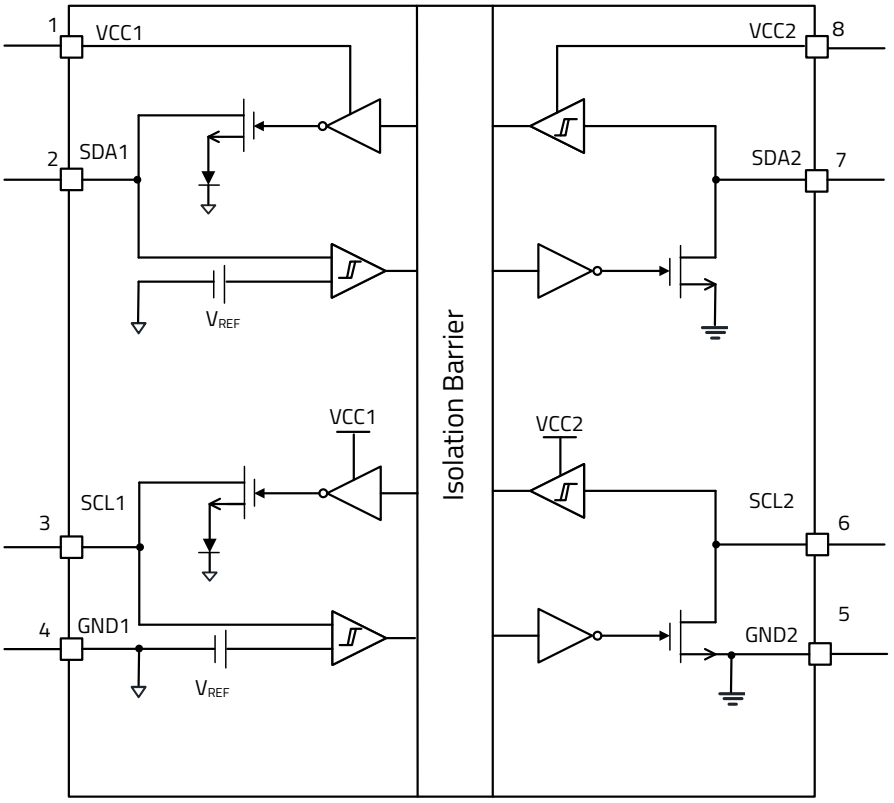


Figure 13: 18032011 block diagram.

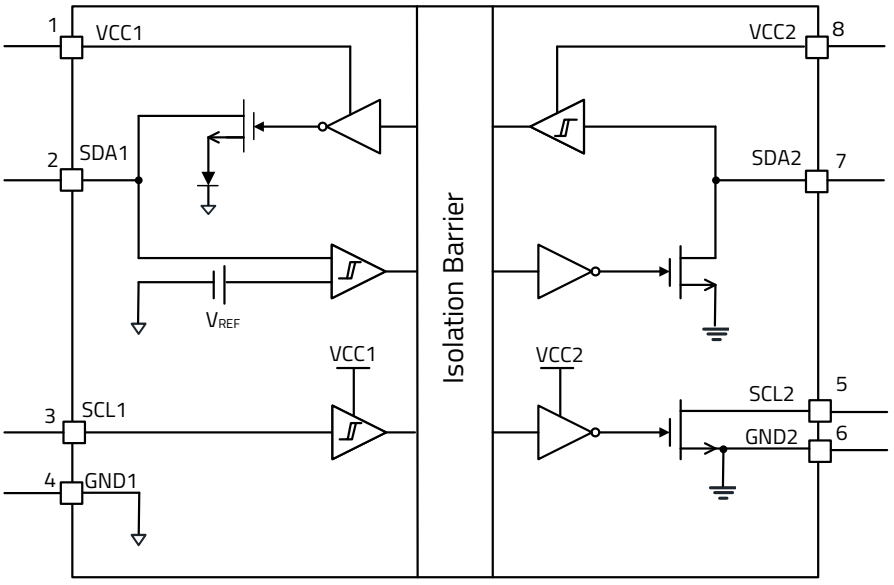


Figure 14: 18032111 block diagram.

16 CIRCUIT DESCRIPTION

The WPME-CDI2C I²C isolator consists of two capacitive isolated channels which transmit the data through silicon dioxide isolation barriers. 18032011 block diagram shows two bidirectional channels with open-drain outputs. 18032111 block diagram depicts one bidirectional and unidirectional channels with open-drain outputs. For raising the bus voltage to high-level, external pull-up resistors need to be connected at both sides.

The special transmitters and receivers on side 1 of bidirectional channels ensure the latch-up protection while regulating the low-level voltage at around 700mV. The Schmitt triggers differentiate between the low-level voltages of input and output based on low-level voltages at side 1 pins (SDA1 and SCL1). It prevents side 1 output low-levels from being retransmitted to the side 2. The side 2 uses conventional transmitters and receivers without low-level logic regulation. A low-level logic on one side pulls the corresponding pin low on the other side without internal data latching.

17 PROTECTION FEATURES

17.1 Supply Undervoltage Lockout (UVLO)

The I²C isolator incorporates input and output supply undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the UVLO are indicated in the ELECTRICAL SPECIFICATIONS. When an undervoltage event is detected on either of the supplies (VCC1 ≤ 1.95V or/and VCC2 ≤ 1.95V), all bidirectional outputs become high-impedance and are pulled high by the external pull-up resistor on the open-drain outputs.

18 TYPICAL APPLICATION

The figure below depicts a typical application of an I²C isolator, 18032011, that provides the required level of galvanic isolation and bidirectional communication between a microcontroller and an analog to digital converter (ADC). In addition, the I²C isolator prevents ground loop currents by breaking conductive ground paths between systems operating at different ground potentials, improves noise immunity, and ensures stable and reliable operation.

The SDA and SCL pins are open drain and require external pull up resistors connected to the respective local supply rails on each side of the isolation barrier. The pull up resistors define the logic high level on the bus by pulling the SDA and SCL pins to the supply voltage when no device is actively driving the lines low. The pull up resistor values must be selected to meet the device sink current capability and the rise time requirements of the I²C bus. The minimum pull up resistance is limited by the maximum allowable low level sink current, while the maximum pull up resistance is determined by the total bus capacitance and the maximum rise time specified for the selected I²C operating mode. In typical applications, pull up resistor values between 2.2kΩ and 4.7kΩ provide an appropriate balance between power consumption and signal integrity.

Each supply voltage pin should be locally bypassed with a recommended 1 µF ceramic decoupling capacitor placed as close to the device supply pin as possible to ensure stable operation and minimize noise coupling.

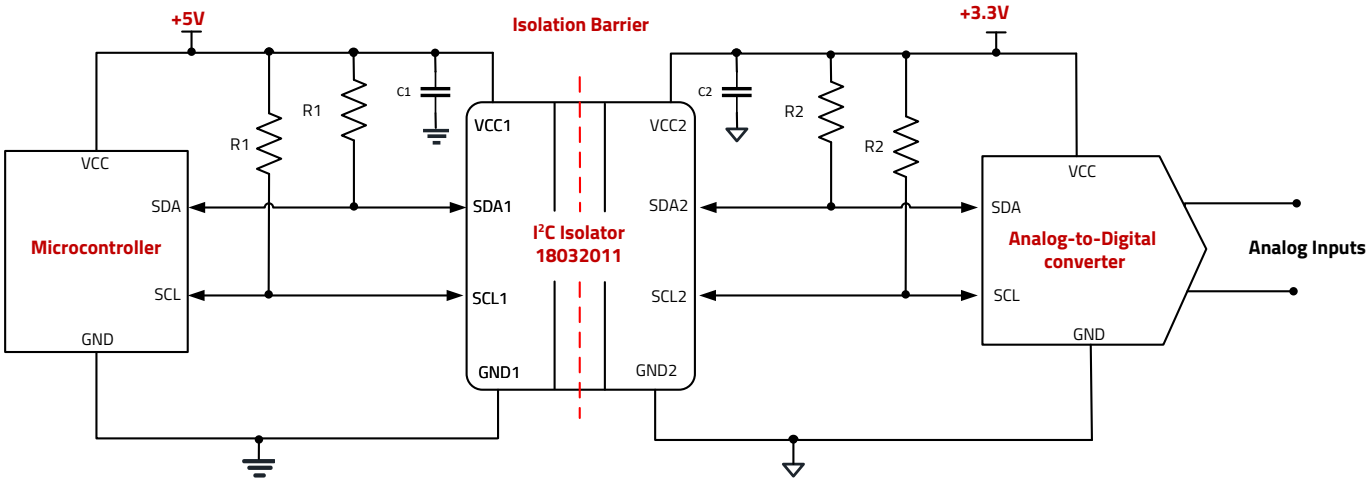


Figure 15: Typical application: Isolated I²C communication for ADC applications.

19 HANDLING RECOMMENDATIONS

1. The I²C isolator is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for the color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of soldering cycles is two.
6. For minimum risk, solder the device in the last solder cycle of the PCB production.
7. The component lead material is copper (Cu) and the lead finish is Matte Tin (Matte Sn).
8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

19.1 Soldering Profile

Table 16: Reflow solder profile.

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150 °C
Preheat temperature maximum	T_{s_max}	200 °C
Preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidus temperature	T_L	217 °C
Time maintained above T_L	t_L	60-90 seconds
Classification temperature	T_C	260 °C
Peak package body temperature	T_P	$T_P \leq T_C$
Time within T_C - 5 °C and T_C	t_P	$t_P \leq 30$ seconds
Ramp-up Rate (T_L to T_p)		3 °C/second maximum
Ramp-down rate (T_p to T_L)		6 °C/second maximum
Time 25 °C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

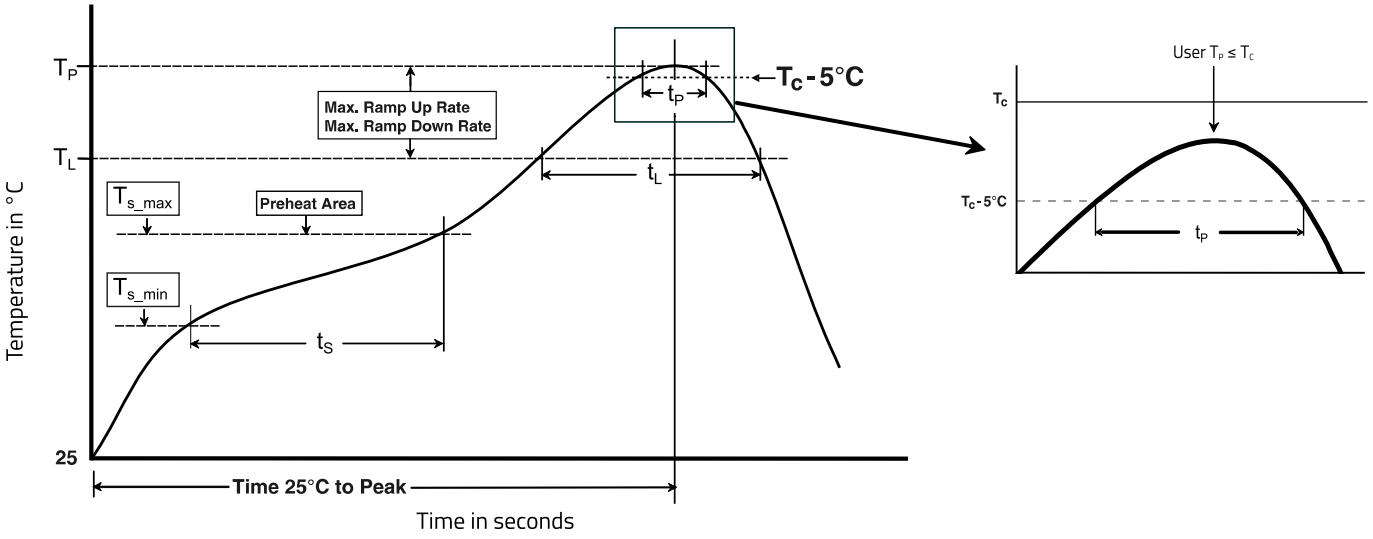


Figure 16: Soldering profile.

20 PHYSICAL DIMENSIONS

20.1 Component

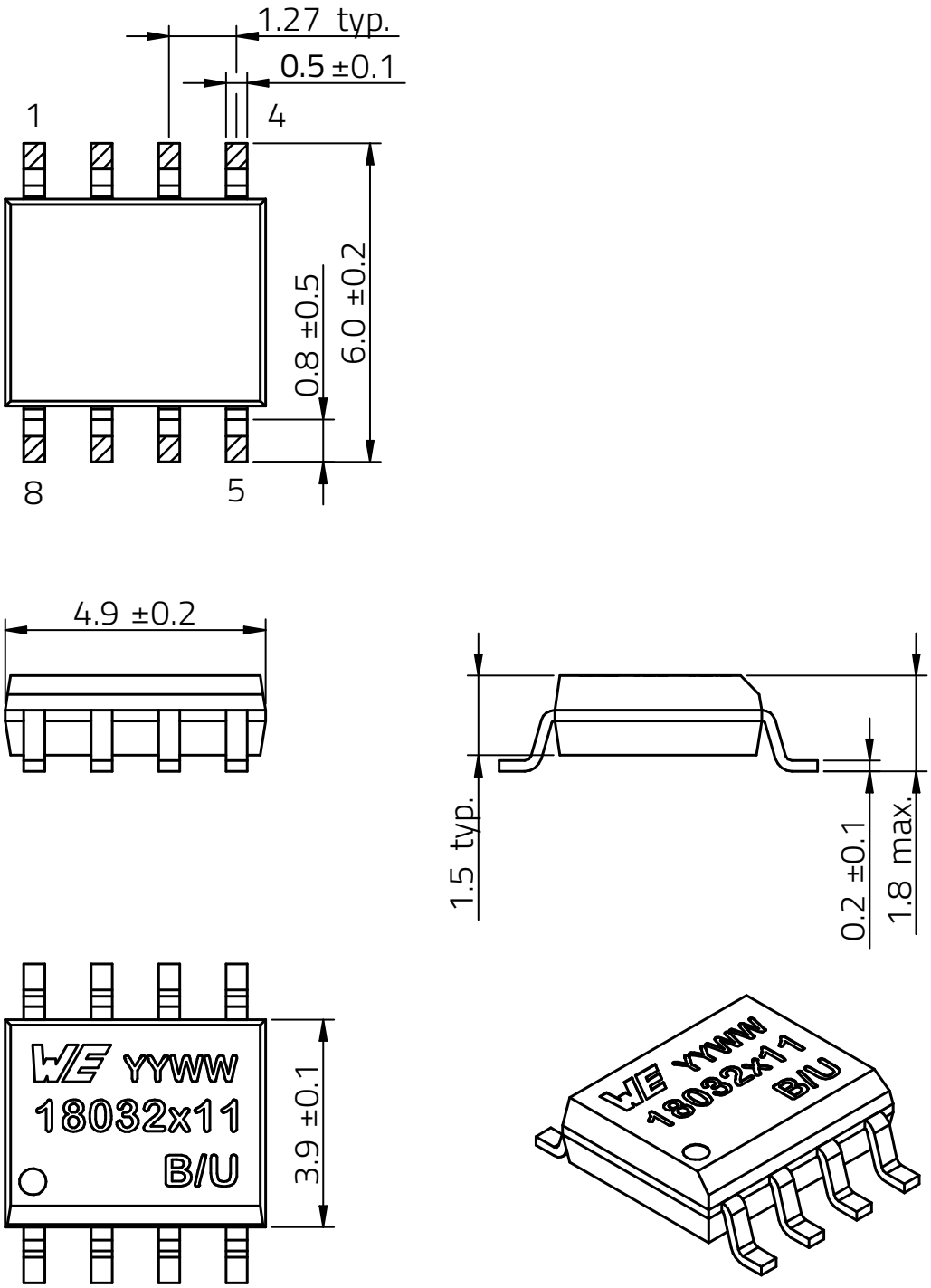


Figure 17: Component dimensions.

All dimensions in mm
Tolerance: xx.x =±0.5mm ; xx.xx = ±0.25mm unless otherwise noted

20.2 Recommended Landpattern

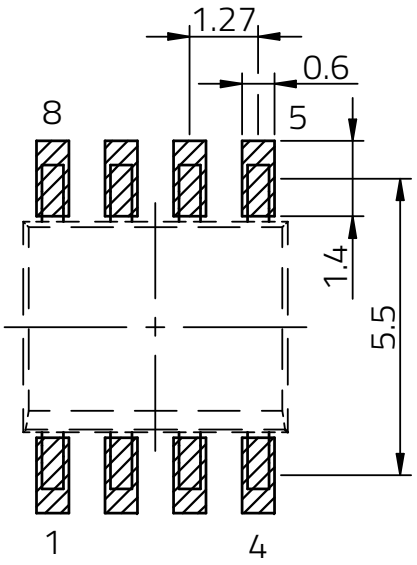


Figure 18: Recommended landpattern dimensions.
All dimensions in mm.

20.3 Packaging

Reel in mm

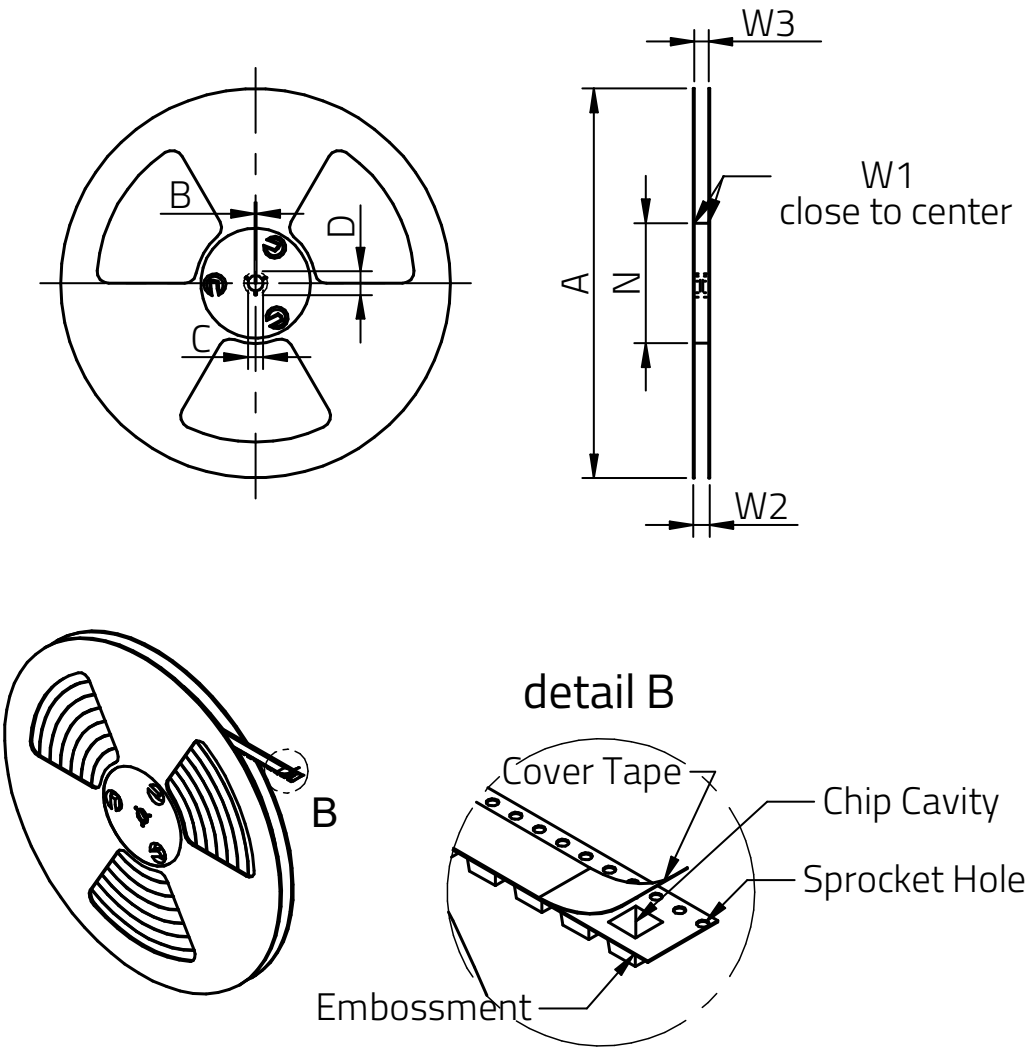


Figure 19: Reel dimensions.

Table 17: Reel dimensions.

A	B	C	D	N	W1	W1	W3	W3
±2.00	min.	min.	min.	min.	+2.00	max.	min.	max.
330.00	1.50	12.80	20.20	60.00	12.40	22.40	15.90	19.40

Reel material is polystyrene.
All dimensions in mm.

Tape in mm

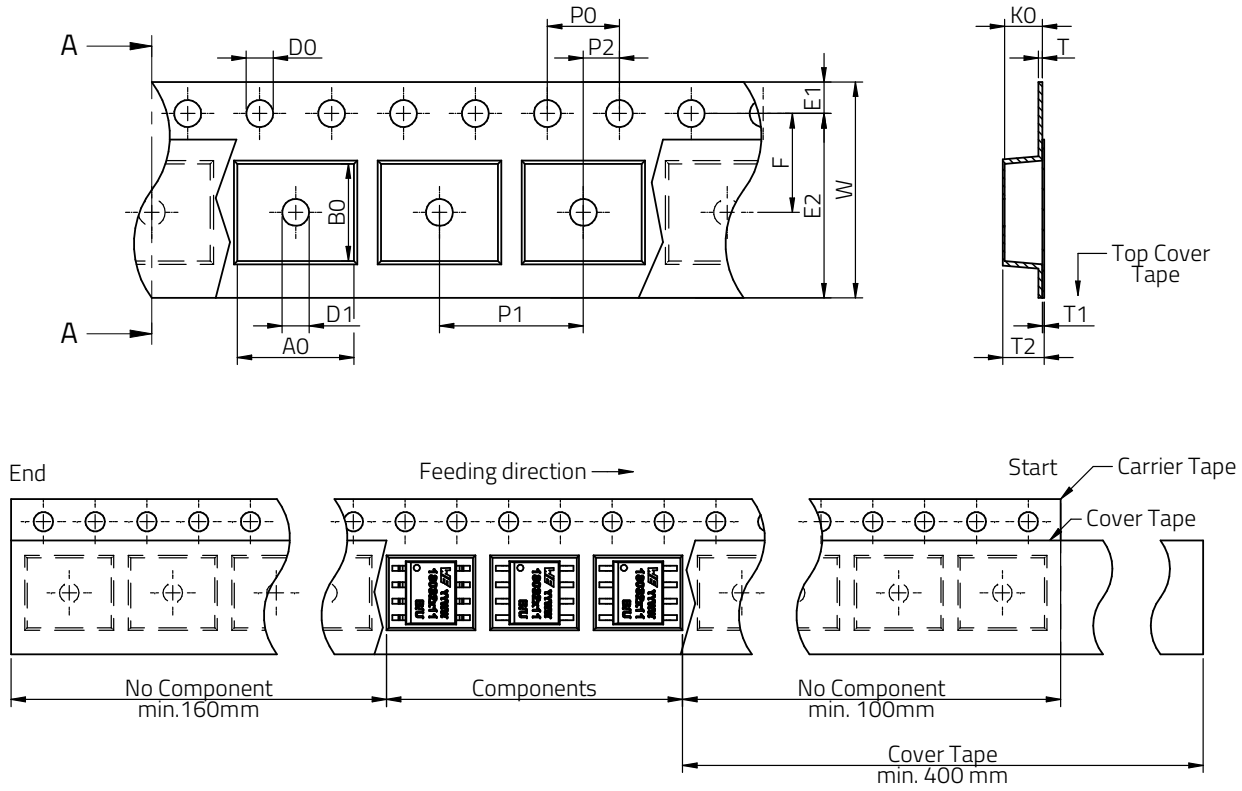


Figure 20: Tape dimensions.

Table 18: Tape dimensions part 1.

A0	B0	D0	D1	E1	E2	F	P0	P1	P2v	W
typ.	typ.	min.	±0.10	min.	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10
6.40	5.40	1.50	1.50	1.75	14.25	7.50	4.00	8.00	2.00	12.00

Table 19: Tape dimensions part 2.

K0	T	T1	T2	W
typ.	typ.	ref.	typ.	typ.
2.10	0.35	0.10	3.40	12.00

Tape material is polystyrene.
All dimensions in mm.

21 DOCUMENT HISTORY

Table 20: Document history.

Revision	Date	Description	Comment
1.0	April 2026	Initial release of datasheet	

22 LIST OF FIGURES

23 LIST OF TABLES

24 CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of digital isolators of Würth Elektronik eiSos GmbH & Co. KG:

General:

- All recommendations according to the general technical specifications of the data-sheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

Product specific:

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

25 IMPORTANT NOTES

General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

Customer Support for Product Specifications

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

Property Rights

All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

General Terms and Conditions

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